# Characterization of a 0.16μm CMOS Technology using SEMATECH ESD Benchmarking Structures

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*Abstract* – A 0.16μm CMOS Technology has been characterized using SEMATECH ESD Benchmarking test structures. The usefulness of the structures is shown with regard to device layout and process issues. Areas where the structures need improvement are also examined.

## I. INTRODUCTION

Test structures are regularly used in the development of on chip protection for integrated circuits. New protection elements are often included on experimental mask sets as test structures to characterize their properties when they are not connected to a full integrated circuit or as an element in an isolated input or output buffer. The characterization of a protection element consists of measuring breakdown voltages, trigger voltages for snapback, holding voltage, maximum current that can be carried before damage, etc. Ideally these measurements should be made at current levels and time scales characteristic of an ESD event. Typically this is done using transmission line pulse (TLP) measurements.[1] Understanding the protection element is only part of the problem of designing an chip protection strategy. The designer needs to know not only the properties of the protection elements being used, but also the properties of the circuit being protected. This requires the full characterization of the technology for ESD robustness.

Failure to characterize an integrated circuit technology for ESD robustness results in a number of problems. Promising protection circuits will not be successful if they do not trigger before a sensitive circuit element. Circuit strategies, which work in one technology generation, may no longer work in a new technology because of subtle differences. Problems can also occur when a product circuit moves from one fabrication facility to another within a company, between a company's internal fabrication facility to a foundry or between foundries.

Full characterization of all, or even a large proportion of the circuit elements of an integrated circuit technology, has not been standard industry practice. The SEMATECH ESD Working Group addressed this by developing a set of test structures for the characterization of a CMOS technology for ESD robustness.[2] The structures are described based on a technology's layout rules making them useful over a number of generations of technology. The SEMATECH ESD working group also published examples of the use of the SEMATECH test structures or structures very similar to the SEMATECH structures.[3] There has not, however, been a comprehensive review of the use of the structures in practice, including an evaluation of their strengths and weaknesses. This paper presents measurements using SEMATECH style test structures for a wide range of circuit elements.

The paper will also address some of the challenges of migrating from a legacy set of test structures to an industry standard set. The ranges of variation of key parameters can be different between legacy structures

and a standard set. This can dictate that extra structures be added to the standard set to provide continuity with earlier data. Experience with legacy structures can also predict that the standard structures include geometries that would lead to poor high current performance. Exclusive use of the standard geometries could result in loss of valuable data. It is not, however, always possible to include both the standard geometry, with its suspected weakness, and a geometry more appropriate for the technology in question. Wafer area constraints, layout resources, and the time and equipment needed for measurement, all dictate that choices sometimes have to be made between strictly following a standard and using a layout which conforms with the spirit of the standard, but with modifications for local use.

# II. MEASUREMENTS

The technology being characterized is a 0.16 μm generation CMOS technology with two physical gate oxide thicknesses of 2.4 and 5.0 nm for 1.5 V and 3.3 V transistors. The technology has silicided gates on which the silicide is formed before gate patterning. Active area diffusions are not silicided. The starting material is 3.2 μm epi on a p+ 100 silicon substrate.

All TLP measurements were made with a non-commercial TLP system with a sub nano-second rise time.[4] All of the measurements used a 100 ns pulse length. Most of the measurements were made in a "high impedance" mode with a 50 Ω termination resistor and a 450 Ω series resistor. In this mode the system has a maximum current limit of 600 mA for a 100ns pulse due to damage to the 50 Ω termination resistor at higher current levels. A limited number of measurements were made in a low impedance mode without the termination and series resistor near the device under test (DUT) but with a diode and 50 Ω resistor at the far end of the transmission line to remove reflections for DUTs with resistances less than 50 Ω. The pulse shapes for the low impedance system were less than ideal, but the measurement results showed good agreement where the measurements overlapped.

The TLP system uses a semi-automated probe station allowing automated measurements over multiple test structures and reticle fields on a wafer. Typically 5 reticle fields on each wafer were measured for each set of test structures. To insure that good contact was made, diodes on each test structure were forward biased and currents measured and recorded. For transistors a limited DC I-V curve was made before each measurement to insure proper functioning of the transistor.

Many of the measurements discussed involve bipolar snapback. The cause of snapback will be discussed later but it is useful to define some of the terms used. Figure 1 shows a simplified I-V curve for a device that displays bipolar snapback. $V_{t1}$, $I_{t1}$ defines the highest voltage and current during avalanche breakdown of a diode before the onset of bipolar snapback. $V_{SB}$ is the snapback voltage, or lowest voltage at which bipolar snapback can be sustained. $V_{t2}$, $I_{t2}$ defines the highest current that can be maintained in bipolar snapback. Sometimes different definitions are used to define this point. Usually it is indicated by a break or kink in the I-V curve that is accompanied by an increase in device leakage. In some devices there can be increased leakage with no corresponding kink in the I-V curve.[5] There are also instances in which there is a very pronounced kink in the curve but excess leakage does not begin until significantly higher currents are forced. It is not possible to define a universal definition of $I_{t2}$. The important point is to describe the criteria being used and to be open to the possibility that an alternative definition may give useful insight.

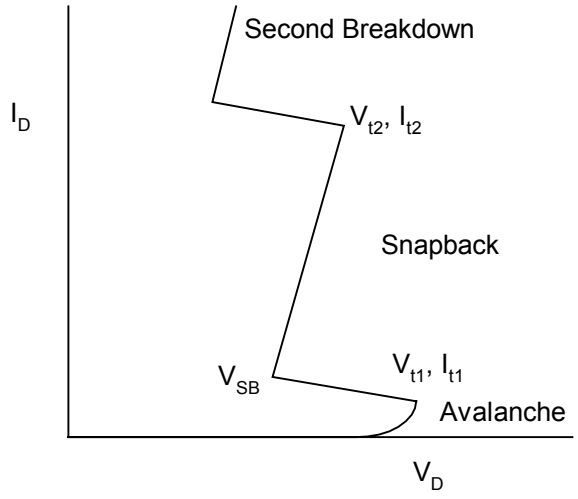


Figure 1: Schematic I-V curve of snapback.

# III. TEST STRUCTURES

The test structures followed the SEMATECH test structure recommendations with some exceptions. For n channel transistors the width variation recommendations were followed, except that several smaller widths were included to provide continuity

with test structures used in previous technologies. Modifications were also made to the well ties recommended in the SEMATECH document. In several structures the SEMATECH guidelines recommended the minimum layout rule separation between the source side of a device and the well tie. Previous experience suggested that that might not be the best arrangement. Rather than use a very close well tie, a well tie separated from the source by 10 μm was used for most of the structures. To allow comparison between the 10 μm separation well tie structures and the SEMATECH recommendation, a limited number of minimum layout rule well tie structures were included. The majority of the structures also used separate pads for the source and well ties, while the SEMATECH document specifies a shared pad for the source and well contacts. Structures were included to test the difference between sharing a pad between source and well tie and having separate pads for the two contacts.

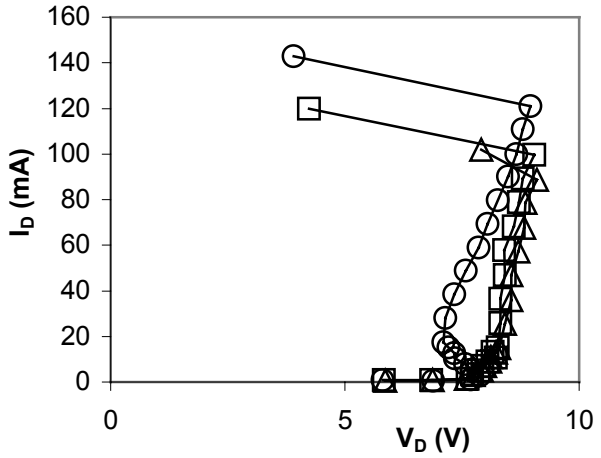


Figure 2: TLP I-V curve of 3.3V pchannel transitors. ○ 10 μm well tie, □ 0.24 μm well tie with separate pads, △ 0.24 μm well tie shorted to the source in metal. All devices are 25 μm wide with a drawn gate length of 0.28 μm. The devices have minimum design rule separation between contacts and the gate. All voltages are negative.

# IV. PMOS TRANSISTORS

P channel transistors receive little attention in the ESD literature. This is likely due to their well-behaved nature, as will be seen in the data. Figure 2 shows examples of p channel transistor I-V curves. The devices are 25μm wide and differ only in terms of their well tie arrangement. One device has a well tie 10 μm from the source contact and uses separate pads for the source and well tie. The other two devices have well ties separated from the source by 0.24 μm, one using separate pads for the source and well tie while the other has the source and well tie shorted in metal at the device. No connection was made to the chuck or substrate. All voltages for the p channel devices are negative voltages but are reported as positive values for ease of presentation. The device with the 10 μm well tie shows a distinct level of bipolar snapback, similar to but not as pronounced as a typical n channel transistor. Neither of the devices with the 0.24 μm well tie separations show the snapback behavior. Any difference between the source and well tie being shorted at the device in metal or shorted together at a common ground point a few centimeters from the devices is fairly subtle.

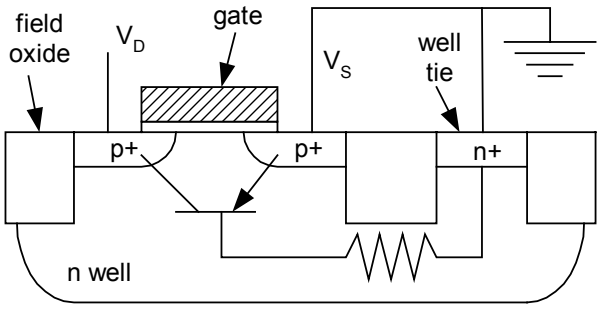


Figure 3: Cross section schematic of p channel MOS transistor showing parasitic pnp bipolar transistor and n well resistor connection to the base of the parasitic bipolar.

The effect of well tie placement for a device in snapback will come up several times in this paper. How well tie placement affects snapback performance is illustrated in Figure 3 for a p channel MOS transistor. All MOS transistors include a built-in parasitic bipolar transistor, a pnp for a p MOSFET, as in Figure 3, and a npn for an n MOSFET. During an ESD event which reverse biases the drain junction of an MOS device, avalanche breakdown will occur in the drain to well junction. For a p MOS device holes will flow to the drain contact and electrons will flow to the well tie. The electron current through the n well resistor will cause the well potential near the source of the p MOS device to drop, which will tend to forward bias the source to well junction. If the voltage across the source to well junction reaches 0.6 to 0.7 V the bipolar transistor will turn on, resulting in a low resistance path between the drain and source of the MOS transistor. The low resistance path, due to the parasitic bipolar action, can result in a drop in voltage between the drain and source of the MOS device, as seen in the TLP I-V curve in Figure 2 for the 10 μm well tie separation geometry. Any factor that affects

the resistance between the well near the transistor source, and the well tie can have an effect on snapback performance. Reduction of the well tie to source separation will reduce the resistance to the base of the pnp bipolar transistor and will make it difficult to maintain the on state of the pnp.

The SEMATECH document calls for p channel widths of 25, 50 and 75 μm. In the current work widths of 10, 25, 50 and 75 μm were used, with a 10 μm well tie separation, as well as widths of 10 and 25 μm with a 0.24 μm well tie separation.

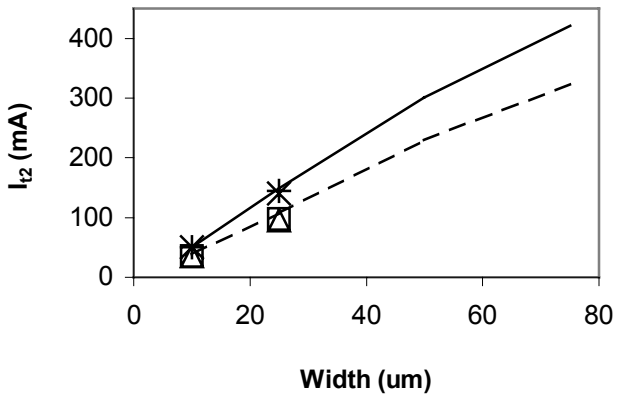


Figure 4: $I_{t2}$ versus width for p channel transistors. Solid line, 1.5V transistors with 10 μm well tie, dashed line, 3.3V transistors with 10 μm welll tie, + 1.5V transistors with 0.24 μm well tie and separate source and well tie pads, X 1.5V transistors with 0.24 μmwell tie shorted shorted to the source, □ 3.3V transistor with 0.24 μm well tie and separate source and well tie pads, and △ for 3.3 V transistor with 0.24 μm well tie shorted to the source. Each point is an average of 5 measurements across a wafer. The drawn channel lengths were 0.16 μm for 1.5 V and 0.28 μm for 3.3 V.

Data for $I_{t2}$ for p channel transistors as a function of width is shown in Figure 4. $I_{t2}$ is defined by a several order of magnitude increase in leakage that occurs during a single pulse. The increase in leakage is usually accompanied by a kink in the I-V curve. The data shows that $I_{t2}$ for a transistor with a well tie 10 μm from the source scales with width, experiencing only a little saturation at the 75 μm width. The transistors with well ties 0.24 μm from the source scale with width up to 25 μm but show a slight decrease in $I_{t2}$ with respect to the devices with a wider spaced well tap.

This data shows that the SEMATECH structures give a reasonable understanding of p channel transistors under ESD level conditions. The SEMATECH test structure recommended well tap geometries did not, however, show the snapback properties which a p channel device can exhibit. The SEMATECH document also recommended variations in coded channel length and multi-finger devices with both of these variations to be at 25μm wide. These variations were not included due to lack of space on the reticle.

# V. NMOS TRANSISTORS

The SEMATECH document describes several variations of n channel transistors including single finger transistors with variations in width, length and contact to gate separation, multi finger transistors, and n channel transistors with built in n well resistors with width and multi finger variations.

In the design of the test structures there was concern about the well tie geometry, similar to that for the p channel transistors. For 25 μm wide transistors, variations were made of well tie separation, with separations of 10, 5, 2, and 0.24 μm with separate contacts for well tie and the source and well tie separations of 2 and 0.24 μm with the source and well tie shorted in metal 1. No differences were seen between the TLP I-V characteristics for any of these variations. The lack of dependence on well tie separation is of interest for n channel transistors, in contrast to p channel transistors where the effect is very noticeable. It is tempting to suggest that the p+ substrate of the p on p+ epitaxial substrate shorts out the p well resistance between the well tie and the source. This is not reasonable because at 0.24 μm and even 2 μm well tie separation to the source, the effect of the substrate should be small with a 3.2 μm epitaxial layer. A better explanation for the difference between the n and p channel devices comes from considering their similar geomitries but differing electrical characteristics. Due to similar geomitries of the n and p channel MOS transistors the base widths of the parasitic bipolar devices will be similar. The doping levels are also very similar. The base resistance for a p channel device will be lower, due to the higher mobility of electrons versus holes. This means that the connection of the well tie to the base is more effective for the p channel device. Coupling the lower resistance of the base contact with the lower gain expected for a pnp bipolar relative to a similarly sized npn it is not surprising that a close well tie can eliminate the snapback of the p channel device but not affect the n channel device.

All subsequent measurements on n channel transistors are on structures with 10 μm well tie separations and separate contacts to the source and the well tie.

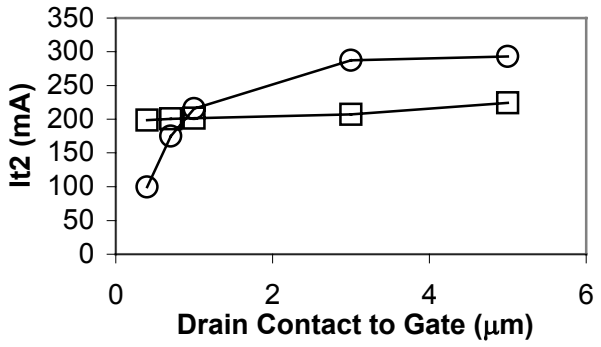


Figure 5: $I_{t2}$ as a function of drain side contact to gate separation for 3.3 V,○, and 1.5 V,□, n channel transistors. Results are average of 5 sites on a wafer. All transistors are 25 μm wide and have drawn gate lengths of 0.16 and 0.32 μm for the 1.5 V and 3.3 V transistors respectively.

All contact to gate separation, as well as length variation in the SEMATECH document is carried out at a width of 25 μm. The document specifies contact to gate separations, of minimum design rule, 1, 3, and 5 μm on the source and drain sides and a single device with 3 μm on the drain side and 1 μm on the source side. Our experience predicted that devices with minimum design rule separation between contacts and gate would have very low current carrying capabilities and would not scale with width. This did not turn out to be a good prediction for a 0.16 μm technology as will be shown below. Because of the expected poor performance of transistors with a minimum separation between contacts and the transistor gate, structures of this type were not included in the test structure set. Previous experience also indicated that increasing the separation on the drain side was more important than source side separation. The final choice of dimensions was for contact to gate separations of 0.4 and 0.7 μm on the drain side with 0.4 μm on the source side and structures with 1, 3, and 5 μm on the drain side with 1 μm on the source side. Measurement results for $I_{t2}$ are shown in Figure 5 where $I_{t2}$ is the maximum current in snapback as defined by a leakage of 100nA. The leakage criterion for failure was chosen for n channel transistors because many of the structures experienced high leakage without a corresponding drop in drain voltage. The expected drop in $I_{t2}$ for small contact to gate separations is clear for the 3.3 V transistors. There is no corresponding reduction in $I_{t2}$ for the 1.5 V transistors. The change in contact to gate separation from 0.4 to 5 μm resulted in an increase in $V_{t2}$ of about 4 V.

To determine what the results would have been for transistors at minimum design rule for contact to gate separation, limited TLP measurements were made on transistor test structures intended for standard DC transistor characterization. These devices were at the same channel lengths as those in Figure 5 but had minimum design rule contact to gate separation. The results continued the trend seen in Figure 5. For 3.3 V transistors, $I_{t2}$ continued its decrease as a function of drain contact to gate separation. The $I_{t2}$ for 1.5 V n channel transistors with design rule contact to gate separation was consistent with an $I_{t2}$ insensitive to contact to gate separation. For widths up to 20 μm, It2 scaled with device width even at the design rule contact to gate separation for both 1.5 V and 3.3 V transistors. These results will not be reported in further detail here because the structures do not follow the SEMATECH guidelines of no shared pads and the widths of metal interconnect were not wide enough.

Based on the above results on contact to gate separation, it is reasonable to follow the SEMATECH guideline of determining length and width dependence of n channel transistors using minimum design rule contact to gate separation. A more complete study can be obtained if devices with wider separation between contacts and the gate are also included.

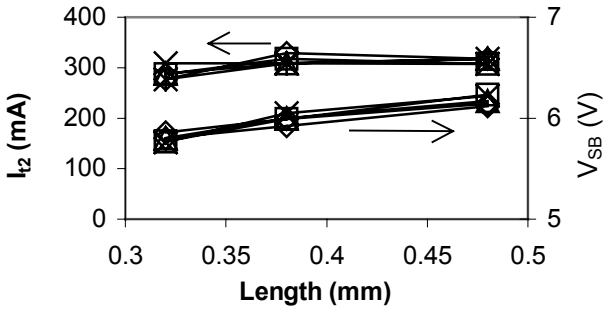


Figure 6: $I_{t2}$ as a function of transistor length for 3.3V n channel transistors.

Due to the expected poor performance of transistors with minimum contact to gate separation,[6] length variations were made with contact to gate separations of 3 μm on the drain side and 1 μm on the source side. Lengths of 0.32, 0.38, and 0.48 μm were chosen for 3.3 V transistors which correspond to the SEMATECH specification of 1, 1.2, and 1.5 times the minimum channel length. Sample $I_{t2}$ data for 3.3 V transistors is shown in Figure 6. The dependence of $I_{t2}$ on channel length is seen to be weak. Also shown in Figure 6 is the snapback voltage, $V_{SB,}$ , for the same

devices. The fairly weak dependence of $V_{SB}$ on channel length shows that the bipolar characteristics of the parasitic npn bipolar transistor formed by the nMOS transistor is not substantially changed by the channel length in this range. This makes the weak dependence of $I_{t2}$ on channel length reasonable.

Data was also taken for 1.5 V transistors as a function of length for 25 μm wide devices. The data is not presented here because the non-linear behavior seen for wide transistors, as will be reported below, is fairly severe for a 25 μm wide, 1.5 V devices.

The SEMATECH document calls for 25, 50 and 75 μm wide transistors drawn at minimum channel length. Due to previous experience with structures at 5, 10, 15, 25 and 50 μm the additional narrow widths were added to the structures studied. The benefit of the narrow devices will become apparent when the non-linear behavior with width is seen for wide devices. It is also easier to make voltage measurement on narrow devices since current levels are lower at critical transition points, such as Vt2, resulting is less ringing in the voltage signal. As with the length variation structures, the contact to gate separation was set at 1 μm on the source side and 3 μm on the drain side. The channel lengths are the design rule lengths of 0.16 and 0.32 μm for the 1.5 and 3.3 V transistors respectively.

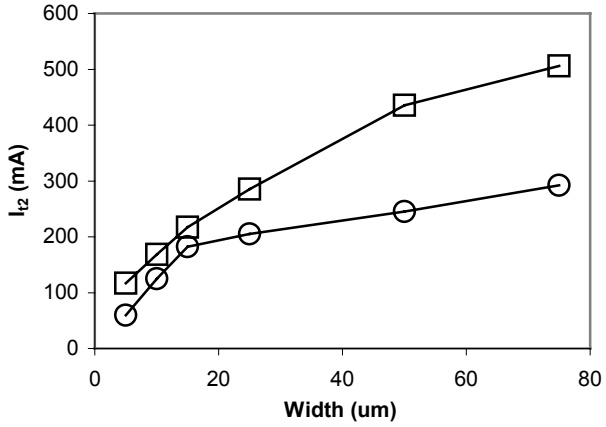


Figure 7: $I_{t2}$ as a function of width for n channel transistors. □ 3.3 V, ○ 1.5 V

Figure 7 displays measurements of $I_{t2}$ as a function of width for both 3.3 V and 1.5 V n channel transistors. The results show clear non-linearity for the wide channel transistors, with the most severe non-linearity for the 1.5 V transistors. Failure analysis showed the failures preferentially near the contacted end of the gate for the wide transistors. No process issue was seen in the failure analysis that would indicate why the failure should occur near the side of the device where the gate contact was made. HBM measurements on the same structures are shown in Figure 8. For HBM measurements the test structures were packaged in 20 pin DIP packages and the source, gate and well tap were shorted together. The failure criterion was a drop in voltage for a 1 nA leakage. The HBM passing voltage clearly scales with device width. This supports the view that there is not an intrinsic non-uniformity in the devices. This result either calls into question the correlation of TLP measurements with HBM or indicates a problem with the TLP measurements as they were performed for n channel transistors.

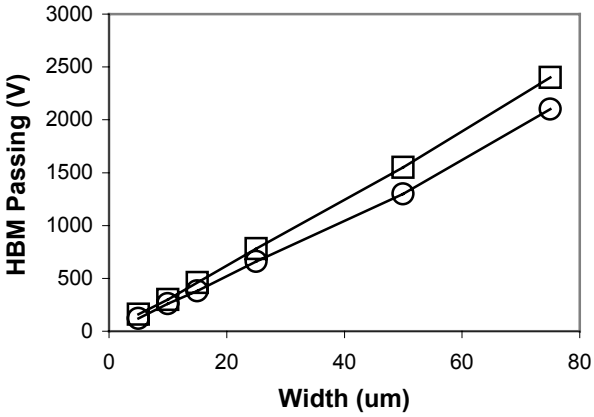


Figure 8: HBM measurements of n channel transistors. □ 1.5 V transistors, ○ 3.3 V transistors

The SEMATECH document calls for a separate pad for the gate. In the measurements made here the gate voltage was driven by an SMU on an HP4156 parameter analyzer. This allows TLP measurements to be made at a variety of gate voltages and allows a simple DC I-V measurement as part of the standard TLP measurement sequence. This presented no problem in the p channel measurements. It is likely that during the fast TLP rise time capacitive coupling of the drain to the gate disturbs the gate potential. The time response of the gate potential to the capacitive coupling is likely to be non-uniform, due to the resistance of the gate, especially for the narrower gate of the 1.5 V transistor. The capacitance and inductance of the long cable connected to the gate could exacerbate this.

To test how the cable and connection to the SMU effected the measurements the gate was shorted to the source with the use of focused ion beam, FIB, techniques on two sets of 1.5 V n channel transistors.

The results of TLP measurements on the modified devices are shown in Figure 9. The results are quite linear. The few points, which do deviate from the straight line, are likely due to damage to the device by charging during the FIB processing. Some of the devices did show some degradation in their properties from the FIB processing but the general results were very good.

These results suggest that the SEMATECH document should specify that the device gate be shorted in metal to the source for TLP measurements with a grounded gate. Additionally, any measurements requiring independent control on the gate voltage should be made on narrow transistors, in the 5 to 15 μm range, to reduce non-uniform gate coupling effects.

Multi finger 3.3 V n channel transistors were also studied. 25 μm wide devices with single, two fingers and 4 fingers were measured with a low impedance TLP system. Two contact to gate separation geometries were studied. Both geometries had 1 μm separations on the source side while the drain sides had 1 and 3 μm separations. In both cases $I_{t2}$ scaled linearly with the number of fingers.

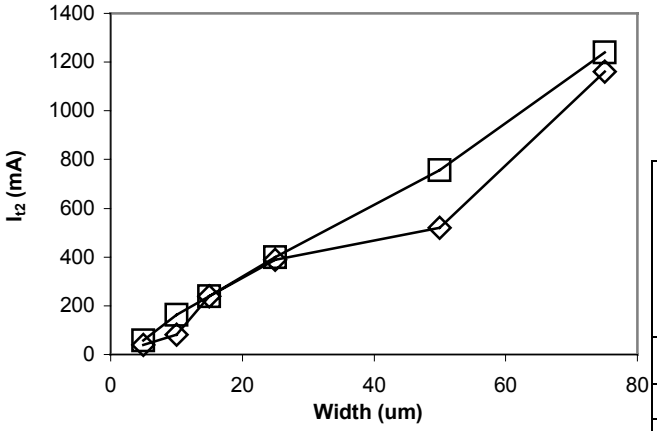


Figure 9: $I_{t2}$ as a function of width for 1.5 V n channel transistors with gate shorted to the source.

# VI. SNAPBACK DEVICE

The parasitic bipolar transistor formed by two closely spaced n+ diffusions separated by field oxide has often been used as a protection element. This device is sometimes referred to as a snapback device. In the SEMATECH document it is referred to as a non-gated thick oxide device. The SEMATECH document calls for widths of 25, 50 and 75 μm, variation of n+ diffusion to n+ diffusion of minimum design rule and 1.5 and 2.0 times design rule, and contact to edge of n+ diffusion of 2, 4 and 6 times the minimum design rule. The document also calls for a minimum design rule separation of a p well tie to the grounded side of the snapback device. The p well tie and the grounded, or source, side of the snapback device are to be shorted in metal. As in the p and n channel transistors this layout raised concern from previous experience with well tie placement. A variety of well tie separations were tried. In some cases the source and well tie were connected to separate pads and in other cases the source and well tie were shorted together in metal.

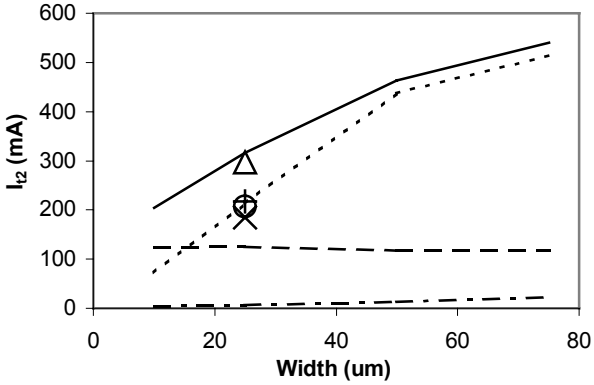


Figure 10: . Five site averages of $I_{t2}$ for snapback devices of various geometries. Table 1 explains symbols.

Table 1: Legend for Figure 10

| | It2 Criteria | Well Tie Separation (μm) | Source and Well Contact | Contact inside n+ diffusion (μm) |
|---|---|---|---|---|
| ····· | Kink | 10 | Separate | 2.00 |
| ——— | Leak. | 10 | Separate | 2.00 |
| - - - - | Kink | 0.24 | Separate | 0.72 |
| – – – – | Leak | 0.24 | Separate | 0.72 |
| + | Kink | 10 | Shorted | 2.00 |
| Δ | Leak | 10 | Shorted | 2.00 |
| × | Kink | 10 | Shorted | 0.72 |
| O | Leak | 10 | Shorted | 0.72 |

There was also concern during layout of the structures that the widest contact to diffusion edge of 6 times the minimum design rules was too small and many of the structures were laid out with a 2 μm contact to diffusion edge. 5 site averages of $I_{t2}$ are shown in Figure 10 for various snapback device geometries. The geometries are explained in Table 1. For the

snapback devices the kink in the I-V curve characteristic of second breakdown and the onset of significant excess leakage were not always closely related. The onset of significant leakage often occurred well after a kink in the I-V curve. For this reason two criteria were used for $I_{t2}$. Both are shown in Figure 10. One is a kink in the bipolar snapback part of the I-V curve. The second is leakage of 0.1 μA.

The data in Figure 10 for 0.24 μm well tie separation shows no dependence on width and carries very little current without damage. The value of the kink defined $I_{t2}$ is so low because there are usually no data points that can be considered to be characteristic of bipolar snapback. The devices go between a state of avalanche breakdown directly to a damaged state, but at a leakage level less than the 0.1 μA level chosen as the leakage criteria. Several geometry variations, including n+ to n+ diffusion spacing and contact inside of n+ diffusion distance, having a separation of the well tie from the source side of the snapback device of 0.24μm were tested. The data from these devices is not shown but all showed very low It2. The devices with 10 μm well tie separations showed much better performance.

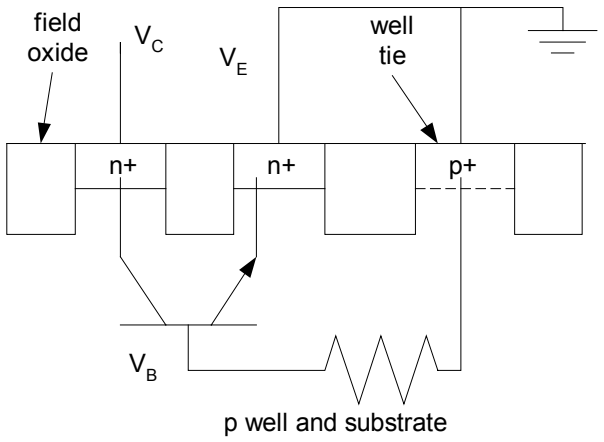


Figure 11: Cross section schematic of a snapback device showing the parasitic npn bipolar.

The reason for the improved performance with wider spaced well ties is similar to the discussion of well ties in a p channel transistor. A cross section of the snapback device is shown in Figure 11, showing the parasitic npn bipolar transistor. Snapback is initiated by avalanche breakdown of the collector to base diode. Electrons will flow to the collector while holes will flow from the base to the well contact. When high enough current flows through the p well/substrate resistor the emitter to base junction will be forward biased turning on the bipolar transistor. If the well/substrate resistance is too low it will be difficult to turn on or sustain the on condition of the bipolar. The situation is made more difficult because of the poor bipolar geometry caused by shallow trench isolation where the emitter and collector are well isolated.

Devices with contacts 2 μm inside the edge of the n+ diffusion and separate source and well contacts showed good scaling with width except for some saturation at 75 μm. For the widest devices, failure due to device leakage at 0.1 μA closely follows a kink in the I-V curve. At 25 μm width there was little difference between shorted and separate contacts to the source and well tie, especially for a kink in the I-V curve. Reduction of the contact to edge of n+ diffusion distance results in a small reduction in current carrying capability in snapback defined by a kink in the I-V curve. The reduction in the contact to n+ diffusion edge resulted in a reduction in the separation between failure defined by a kink in the I-V curve and failure due to leakage at the 0.1 μA level.

# VII. INTEGRATED RESISTOR

The SEMATECH document includes the layout for n channel transistors with an integrated n well resistor. The integrated resistor is formed as shown in Figure 12. The characteristic length of the resistor is formed by the width of the field oxide. This is not the only way to make integrated resistors. Instead of using field oxide to define the resistor length a transistor gate can be used instead[7][8]. The device is sometimes called a gate defined n tub (well) resistor or GDNTR. This is shown in Figure 13. This has two advantages. The well-controlled gate process, rather than the field isolation process, forms the resistor length. Also the current path both during normal operation and during an ESD event includes the full depth of the n well rather than only the limited doping under the field oxide.

The SEMATECH document does not discuss this type of structure. However, the document can provide guidance for the construction of test structures. The document calls for transistor/n well widths of 25, 50 and 75 μm, field oxide dimensions for defining the n well resistor length of 1, 1.5 and 2 μm, and transistor lengths of 1, 1.2 and 1.5 times the minimum design rule. For our use widths of 5, 10, 25, 50 and 75 μm were chosen. The extra widths were included to provide continuity with earlier structures. Gate

lengths of 0.20, 0.24, 0.28, and 0.36 μm were chosen for the GDNTR lengths. These values almost cover the factor of 2 difference called for in the SEMATECH document but are centered closer to our use condition. Transistor length variation was not included due to space restraints.

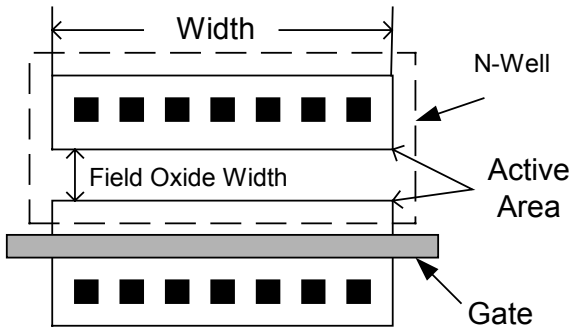


Figure 12: Layout of a field oxide defined n well resistor integrated with an n channel transistor.

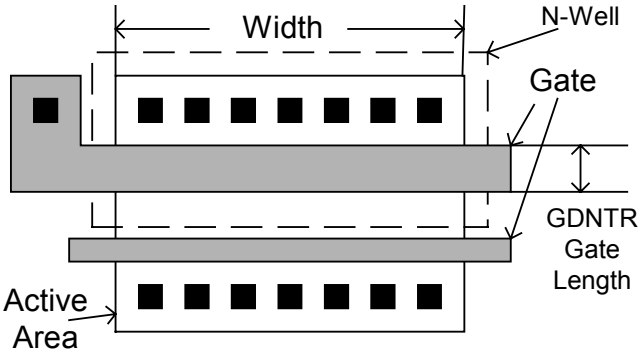


Figure 13: Layout of a gate defined n well resistor integrated with an n channel transistor. The contact to the gate is tied in metal to the contacts to the active area inside the n well.

Samples of the TLP measured I-V curve for a variety of GDNTR lengths are shown in Figure 14. The curves are very similar to those for a transistor alone; showing a transition from a low current region to a snapback region that can carry high currents without damage. The snapback region shows considerable curvature. This is the result of velocity saturation and heating of the resistor during the pulse.[9] The results shown in Figure 14 are from measurements near the end of the 100 ns pulse. If the measurements are taken earlier in the pulse the curvature is less due to less resistive heating. At higher currents the device suffers second breakdown and is damaged. Figure 14 shows that the effect of length variation in the GDNTR length is not strong. The transition to second breakdown is pushed out to higher voltages by the longer resistor, moving from 11.7 V for a 0.20 μm long GDNTR gate to 13.9 V for a 0.36 μm long GDNTR gate. The dependence of $I_{t2}$ on the GDNTR gate length is also weak, changing from 155 mA for the 0.20 μm GDNTR gate length to 140 mA for the 0.36 μm long GDNTR gate.

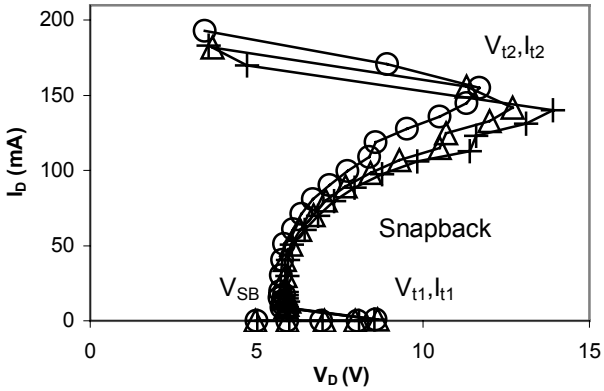


Figure 14: Sample TLP measurements for GDNTR integrated with an n channel transistor. The device is 25 μm wide with GDNTR gate lengths of O 0.20 μm, Δ 0.28 μm, and +, 0.36 μm.

The scaling of current carrying capability as with width is very important for an ESD protection element. Figure 15 shows the current carrying capability for GDNTR devices in series with n channel transistors as a function of width. Two failure criteria have been used. One is the kink in the I-V curve shown by the point $V_{t2}$, $I_{t2}$ in Figure 14. The second is the onset of a particular level of leakage, in this case 100 nA. Showing two failure criteria has been done because GDNTR devices in series with n channel transistors often will fail to show excess leakage, even when the I-V curve shows the characteristic features of second breakdown. Figure 15 shows that for narrow devices there is considerable difference between the two failure criteria. For wide widths the two failures occur at almost the same current level.

The failure of the GDNTR device to show leakage closely associated with the kink in the I-V curve is likely due to the depth of the n well resistor. Damage can occur without the damage crossing the deep n well junction. This effect can also be seen in HBM data. Figure 16 shows HBM data from packaged GDNTR - n channel transistor test structure from the same lot as shown in Figure 15. A drop in the voltage required for a 1 nA leakage determined an HBM failure. The HBM results for narrow devices show a weaker than linear dependence on width. Only for the wide devices does the behavior approach a linear dependence on width. This closely mimics the

behavior of the TLP data when a leakage criterion is used for failure.

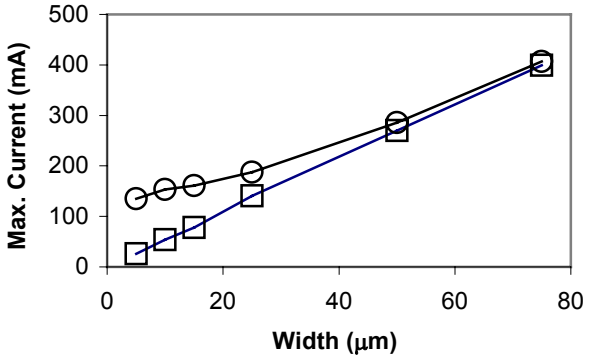


Figure 15: Current carrying capability of GDNTR in series with an n channel transistor as a function of width. Points are the avarage of 4 sets of data on a wafer. □ $I_{t2}$ defined by kink in I-V curve, ○$I_{t2}$ defined by 0.1 μA of leakage.

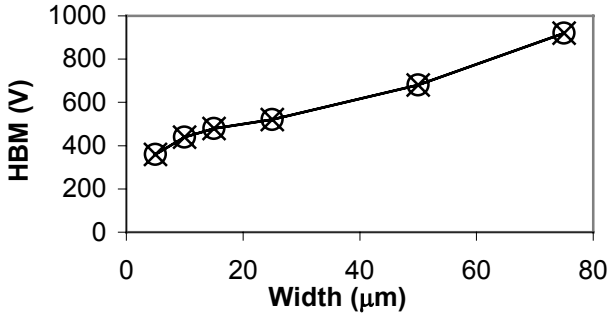


Figure 16: HBM data for two sets of packaged test structures of GDNTR in series with n channel transistors.

# VIII. CONCLUSIONS

The SEMATECH structures have proven useful in understanding the ESD characteristics of a 0.16 μm CMOS technology. There are several areas where the SEMATECH test structure document may need modifications. Foremost among these are well tie separation for p channel devices and especially snapback devices. The handling of the connection to the gate of n channel devices needs to be addressed more carefully.

# IX. Acknowledgements

We would like to thank David Shuttleworth for help with the failure analis, Stephen Brown for the FIB work, Mike Carrol for helpful discussions and Pascal Salome for useful suggestions on the manuscript.

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