Standardization of the Transmission Line Pulse (TLP) Methodology for Electrostatic Discharge (ESD)

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In Memory of Hugh Hyatt

Abstract **-** Standardization of the methodology of transmission line pulse (TLP) testing has become a necessary reality as it becomes a common place practice in the ESD discipline. This paper discusses the development and method of a TLP standard practice.

I. Introduction

As the desire to provide better understanding of the electrostatic discharge (ESD) robustness of electronic components increases, a larger focus on better ways to diagnose and characterize devices or systems is occurring with the introduction of transmission line pulse (TLP). TLP testing is a rapidly growing practice and discipline in electronic components and systems. Only in recent times has the popularity and proliferation of the TLP method for ESD testing has grown from the laboratory to a commonplace diagnostic tool for ESD, failure analysis, and circuit design engineers. In this paper, a standard practice for TLP testing will be discussed. The publication will discuss the evolution of TLP standard practice (SP). Topics on TLP testing, such as different classes of systems, pulse waveforms, required equipment, test procedure, calibration, verification, leakage and failure criteria, will be reviewed.

II. Purpose

Interest in TLP testing is growing rapidly in the testing of electronic components in the semiconductor industry. TLP testing techniques are being used for semiconductor process development, device and circuit design. This technique or practice is being utilized on products in both wafer level and packaged environments. TLP testing is used as an ESD characterization tool to obtain voltage-current pulse characterization parameters, failure levels, and ESD metrics. Early studies of pulsed phenomena were initiated for military applications for electromagnetic pulse (EMP) phenomena [1-3]. In the late 1960's and early 1970's a larger interest was evident in the semiconductor industry in the evaluation of the power-to-failure of semiconductor components to pulsed phenomenon [1-3]. It was not until the 1980's that this method was re-introduced and popularized for wafer-level semiconductor components and circuit model development [4-5]. The TLP technique is being used today for ESD devices and circuits for CMOS, silicon-on-insulator (SOI), and BiCMOS silicon germanium (SiGe) technologies [6-18]. Thus, the TLP system is to the ESD engineer what the semiconductor "parameter analyzer" is to the semiconductor engineer.

The question of the necessity to have a TLP standard for ESD testing was first addressed by the SEMATECH Quality and Reliability Council ESD working group. At that time, the belief was that it was too early to establish a TLP specification, but a best methods or standard practice would serve the semiconductor industry. It was also believed that it was possible that TLP testing may change the

paradigm on how we test, characterize and qualify semiconductor processes and components for ESD phenomenon and reliability. A TLP survey, sent to over 30 TLP engineers, showed significant consensus and commonality of methodology was being used today as well as a sentiment that the industry needs a "best methods" or standard practice document.

At the onset of establishment of a TLP SP document, the majority of TLP systems were designed by engineers in a laboratory environment. No commercial TLP systems were available in the industry nor was TLP data provided to customers. With the emergence of commercial TLP systems, it became clear that a TLP SP or specification was needed for TLP vendors, the semiconductor industry and product customers. With the usage of TLP data for ESD characterization and product quality evaluation, there is a growing need to have standard methodologies, failure criteria, and means of reporting to allow dialogue among semiconductor suppliers, vendors, and product customers. A methodology used by electrical technicians, electrical engineers, semiconductor process and device engineers, ESD reliability and quality engineers, and circuit designers will provide value to the industry as an educational guide, a learning document, and as a reference for the practice being used today. For the ESD industry, the purpose of a TLP SP is to provide a common method to allow comparison of experimental data and test methodology which will enable a means to provide common interpretation. In doing this, a foundation of communication is established for dialogue and a future TLP test standard for the semiconductor industry.

Today, the context is the application of TLP techniques for the electrical characterization of semiconductor components. These semiconductor components can be single devices, a plurality of devices, integrated circuits, or semiconductor chips. This methodology is relevant to both active and passive elements. Although the scope and focus of TLP techniques pertains toward semiconductors, this does not preclude usage of this method to other higher-level elements.

III. TLP System Configurations

TLP systems can be classified according to their configuration; these can include the current source, time domain reflectometry (TDR), time domain transmission (TDT), and time domain reflection-transmission (TDRT) configurations. These systems vary in the configuration of the transmission lines (TL), current and voltage probe, attenuators, and resistor elements as well as whether the incident, reflected or transmitted waveform is measured.

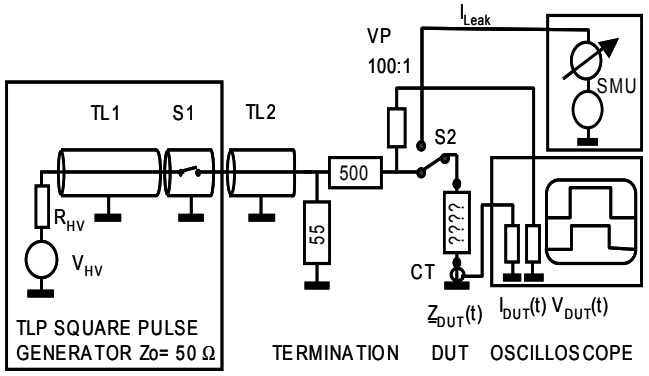

Figure 1: TLP Current Source Configuration.

Figure 1 shows the TLP current source configuration. A high voltage source charges a transmission line through a high impedance resistor whose value is on the order of 10MΩ. When the TL is charged, the switch S1 is open. The TLP square pulse generator impedance is typically 50 Ω. A switch S1 is in series with the first source TL followed by a second TL. A 55 Ω resistor is tied to ground in parallel with the 500 Ω resistor element and the device under test (DUT).

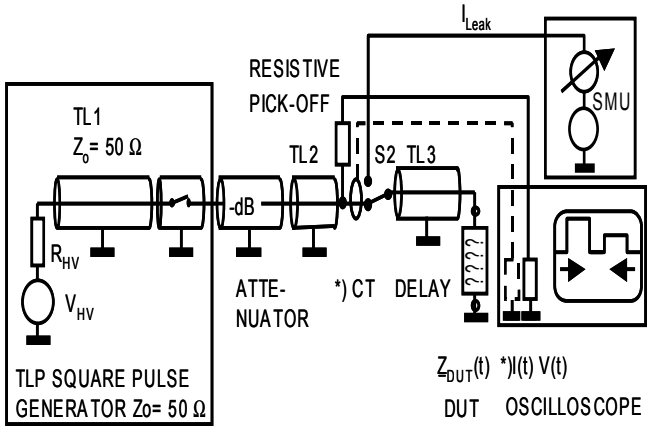

Figure 2: Time Domain Reflectometer (TDR) TLP with attenuator for re-reflected stress pulses.

Figure 2 is a second TLP configuration, which will be referred as a Time Domain Reflectometer (TDR) TLP system. As in the current source TLP system of Figure 1, the source configuration, its method of charging, and first switch S1 are equivalent as indicated by the left hand box. In this TDR system, it is followed by an attenuator and second TL (TL2). In this

implementation, the voltage and current are measured not at the DUT but between TL2 and TL3. The incident pulse and the reflected pulse waveform are then evaluated. The leakage current is evaluated between TL2 and TL3 using switch SW2.

Figure 3 shows the Time Domain Transmission (TDT) TLP system. In this configuration, the oscilloscope measures the pulse waveform which is transmitted past the DUT. The signal is sent from the TLP square pulse generator through the attenuator (1). This signal is then propagated to the DUT by closing of switch S2.

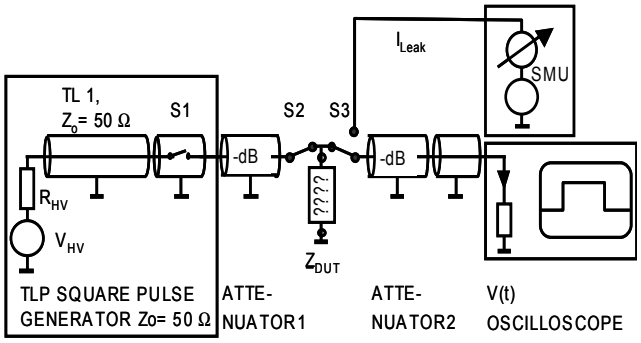

Figure 3: Time Domain Transmission (TDT) TLP system without attenuation of stress pulses reflected from the open end of the TL1.

The transmitted signal passes through attenuator(2) to the oscilloscope. Hence in this method, the transmitted pulse signal is measured at the oscilloscope instead of the incident or reflected pulse.

In Figure 4, a fourth configuration exists which can evaluate both the transmitted and reflected wave. This is known as a Time Domain Reflection and Transmission (TDRT) TLP system. In this configuration, as in the TDT system, the transmitted signal is measured by the oscilloscope. A distinction in this system is that the transmitted signal passes through the DUT since it is in a series configuration. Additionally, the reflected wave is measured at the source end. In this case, there is no attenuation of the reflected pulse signal.

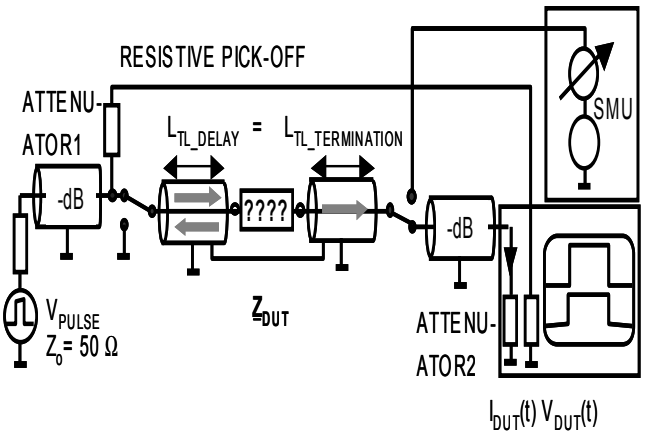

Figure 4: Time Domain Reflection & Transmission TLP (TDRT) without attenuation of the re-reflected stress pulse

Table 1 summarizes the different TLP-systems in terms of impedance, symmetry with respect to earth, multiple reflections and the measured quantities of voltage and current as well as the position where they are measured.

Table 1: Overview TLP-Systems

Transmission Line Pulse Tester Systems				
Current Source >20 ns	**Constant Impedance > 2 ns**			
CS	**TDR**		**TDTR**	**TDT**
Unbalanced 500 Ohm	Unbalanced 50 Ohm	Balanced 100 Ohm	Unbalanced 100 Ohm	Unbalanced 50 Ohm
Reflections: Minor	(Multiple) Reflections → attenuator or diode required			
$I_{DUT}(t)$ & $V_{DUT}(t)$ measured close to DUT	$V_{DUT}(t)$ and opt. $I_{DUT}(t)$ measured remotely		V_{DUT} & I_{DUT} measured remotely	V_{DUT} $V_{reference}$
	If incident and reflected pulses are overlayed the incident pulse must be very repeatable and flat			Pulse must be very repeatable !

IV. Pulse Waveform Requirements

An important step of establishment of a TLP standard practice is the pulse waveform requirements. The pulse waveform requirements include the pulse width, rise time, fall time, maximum overshoot, ringing duration, and measurement time window. Load condition requirements are addressed for evaluation will be reviewed.

The voltage and current conditions for the waveform are dependent on the load conditions.

Table 2. Pulse Waveform Parameters

Pulse Parameters	Value	Load
Current Pulse Width	100 ns	Short
Voltage Rise Time	0.2 to 10 ns	Open
Current Rise Time	0.2 to 10 ns	Short
Fall Time	Greater or equal to rise time	N/A
Maximum Peak Voltage Overshoot	20% of plateau	Open
Maximum Voltage Ringing Duration	25% of pulse width	Open
Maximum Peak Current Overshoot	20% of plateau	Short
Maximum Current Ringing Duration	25% of pulse width	Short
Measurement Time Window	10% to 95% of pulse width	N/A

From the TLP survey, the majority of users of TLP systems today use a 100 ns pulse width. This pulse width is typically chosen to be equivalent to an HBM type event (with respect to the power-time domain). The voltage rise and fall times were typically less than 10 ns. For the overshoot condition, the majority of test systems could establish an overshoot less than 20% of the current or voltage plateau of the TLP pulse. Typically, voltage and current ringing is evident at the front end of a TLP pulse waveform. With proper design and matching, this can be minimized in magnitude and duration. It is important to reduce the current ringing duration in order to find a time regime where an accurate DUT voltage and current measurement can be taken. The time regime in the pulse width where a measurement is taken is the measurement time window. The quality and accuracy of the measurement is dependent on the noise-free nature of this region as well as averaging processes to extract the DUT voltage and current.

Examples of the current and voltage waveforms into open and short circuit conditions are shown (Figures 5 and 6). In the case of the open circuit condition, voltage overshoot is evident at the rising edge of the TLP pulse. In the case of the short circuit, current overshoot is evident at the rising edge of the TLP pulse. In both cases, a well-established plateau is exists allowing for evaluation of the current and voltage in a wide measurement window. In the case of a 100 ns pulse width, this allows for accurate and quality evaluation of the DUT current and voltage.

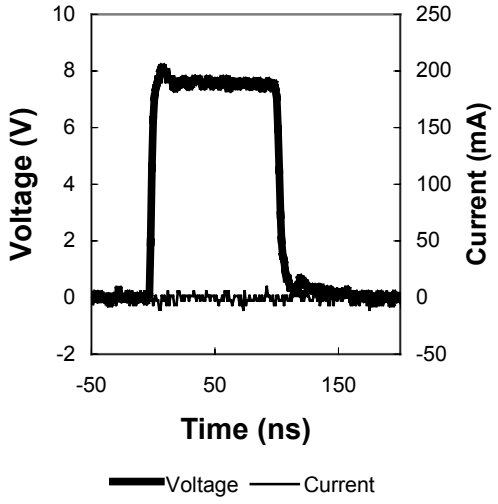

Figure 5. Voltage and current waveform into an open-circuit.

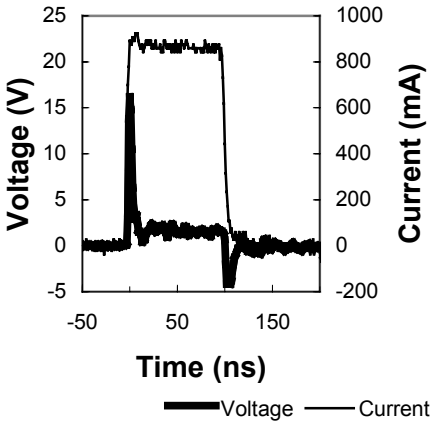

Figure 6. Voltage and current waveform into a short circuit.

V. TLP Test Procedure

The steps of TLP testing are important for proper evaluation of the current, voltage, leakage, and failure process of the DUT. Figure 7 shows the test sequence which includes the steps of calibration and verification, initial leakage testing, application of the stress voltage, measurement and recording of the current and voltage, and leakage measurement.

The TLP test procedure uses a series of increasing pulse amplitudes to characterize or test a device, discrete circuit, or test structure.

This test procedure is described below and illustrates the test flow chart:

- Select appropriate test levels, including pulse width, amplitude and polarity
- Select step size increments.

- Establish a minimum time between successive step pulses of 0.3 s to allow for DUT cooling.
- Define failure criteria. Perform initial (reference) leakage current measurement on the DUT.
- Apply a stress pulse of a fixed width to the DUT. TLP testing should begin at the lowest desired level of interest and increased using the defined step stress.
- Measure and record the stress pulse voltage and current; this will represent one I-V point on the I-V curve.
- Perform a leakage measurement. If the device satisfies the DUT failure criteria, the test is complete.
- Increase the pulse amplitude to the next desired level and repeat method steps to the maximum desired pulse amplitude. This will generate a series of pulses.

Initial leakage current is taken prior to measurement by closing the second switch as shown in the previous discussed TLP system configuration. An initial pulse is applied to the DUT in accordance with the pulse waveform characteristics. For evaluation of the DUT current and voltage value, many measurements are taken within the measurement window which are subsequently averaged. After this measurement process, a switch is closed to evaluate the leakage condition. If the measured leakage current is in excess of the failure criteria, testing is discontinued. In the case that the failure criteria is not achieved, the testing process is continued and the process is repeated with the subsequent step is initiated with transmission line charged to a higher voltage. It is necessary to set the desired step size to magnitudes consistent with the test structure response in order to minimize measurement error. Note that depending on the DUT configuration and requirements, an additional bias can be applied to the DUT terminals during application of the TLP pulse. Ground loops should be avoided to eliminate accidental triggering of the DUT.

A simple semiconductor parametric analyzer can be used for measuring leakage of discrete test structures, but it may not be sufficient for measuring leakages of all circuit types and complex structures. Evaluation may require pre-conditioning or powered states.

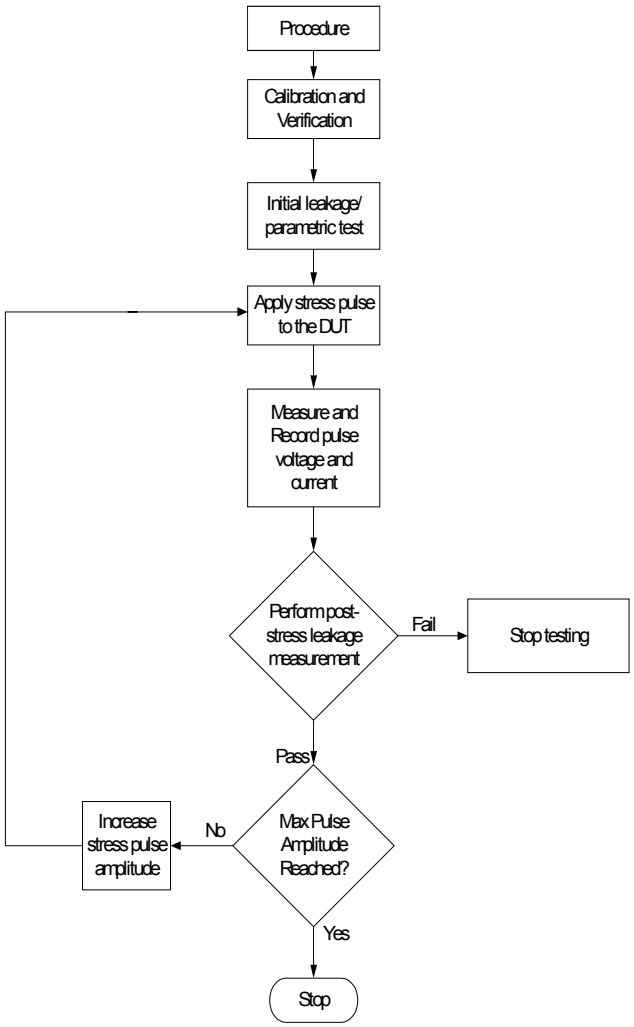

Figure 7. TLP Testing Sequence and Method.

VI. Error Correction, and Verification

Prior to initiation of TLP testing, it is a standard practice to extract the system error from the electrical measurement. This is ensure accurate measurement and nullifies system resistance in the measurement. The "calibration and verification" procedure will be discussed for the system which is performed prior to the measurement process.

Adjustments of both current and voltage measurements are important to remove unavoidable non-ideal system characteristics (e.g. contact, and shunt resistance). Periodic verification using simple components with known properties insures accurate measurements.

The error correction methodology, including the open and short circuit measurements, is performed at least once per shift or when the equipment is modified.

Longer periods between error correction steps may be used if no changes in the error correction factors are observed for several consecutive checks. A separate set of adjustment values is created for each test pulse rise time, or configuration of cables and probes used to collect device data. The adjustments derived from the short and open measurements may be applied to the data within the operating system software, during post processing using spreadsheet or other data analysis software. To insure accurate results, all measurements should be performed on properly calibrated measurement instruments.

A. Error Correction: Short Circuit

Measurements through a short circuit allows with correction for system and contact resistance. The procedure is as follows:

- Connect an electrical short circuit to the end of the device testing connections or wafer probe needles at the DUT. In the case of wafer probes, placing probe needles on a low resistance clean metal pad can be considered as a good electrical short circuit. The short circuit should be made of the same type of material to be used during device measurements or verification, and should be verified by standard low resistance measurement techniques with accuracy to 1 mΩ.
- Perform a TLP test using at least 5 points with the last point set to the maximum current. If the slope of a line through the test points is not zero Ohms, then the value of the slope of the line in V/A (Ω) represents the internal adjustment value and should be used to correct the DUT I-V test data.
- Record the measured V/A values for reference and use until the next short circuit verification.

For the greatest accuracy, use an I-V plot range of +/- 1 V with the current range set to highest value used in the TLP system. In this fashion, measurement error can be reduced.

B. Error Correction: Open Circuit

Measurements through an open circuit allows the correction of shunt resistance contributions. To evaluate, provide an open circuit at the end of the device testing connections for a socket tester. For wafer probing, disconnecting the probe needles with the short circuit will provide an optimum open circuit. The procedure is as follows:

- Perform a TLP test using at least 5 points with the last point set to the maximum voltage . If the slope of a line through the test points is not infinite Ohms, then the value of the slope of a line in (1/ohms) represents the internal adjustment value and should be used to correct the DUT I-V test data.
- Record the measured A/V (or V/A) values for reference and use until the next open circuit verification.
- For the greatest accuracy, use an I-V plot range of +/-10 mA with the voltage range set to the highest value used for device testing.

Typically, the current probe losses inject 1 Ω into the current carrying wire, thus the total V/A correction will be greater than 1 Ω . TLP test leads running to a wafer probe station can add an additional 1 Ω to the V/A error correction (approximately 1 Ω for socket testing and 1 to 2 Ω for wafer testing). Unless a voltage probe with a lower resistance provides greater shunt losses, The V/A error correction will vary in the 10 to 100 k Ω.

C. Verification

Verification of TLP test system accuracy should be performed regularly and prior to system use. The verification procedure and methodology is dependent on the TLP method. Verification can be performed using both a Zener diode and a resistor. The Zener diode is used to verify the system voltage error. Once the voltage error is known, a resistor is used to verify the system current error. A procedure is as follows:

- Measure the dc breakdown voltage of a Zener diode.
- Perform a reverse bias TLP test on the Zener diode above the Zener breakdown voltage. Compare the TLP and d.c. breakdown voltage.
- Choose a resistor whose value is comparable to the DUT resistance. Measure the resistance to within 10 m Ω. A four-wire (Kelvin) technique removes contact resistance from the measurement. For a socket system, insert the resistor into the test socket. For a wafer probing system, place the probe needles on the electrical terminals of the resistor element.
- Perform a TLP I-V measurement. The number of voltage steps should be chosen to minimize measurement error relative to the average resistance straight-line slope. Use the V/A and A/V error correction results to correct for system, contact, and shunt resistance.

- After the test completion calculate the V/A ratio (e.g. slope). Compare the calculated versus measured d.c. resistance (the difference is a measure of the amount of error in the TLP measured resistance). Given the measured voltage has been found to be accurate (e.g. based on the Zener diode measurement), a determination of current measurement accuracy can be obtained by comparing the measured and calculated current. This is based on the measured voltage divided by the known resistance value. Perform the resistance measurement for each rise time and cable configuration to be used.

VII. Example TLP Measurement

A TLP I-V characteristic is a locus of single pulse events where each I-V point represents the recorded current and voltage across the DUT during a pulse test event within the measurement window. Note that this data point may be an average of a set of points within the measurement window; this will be a function of the high frequency variation, noise, number of sample points averaged and width of the sample window.

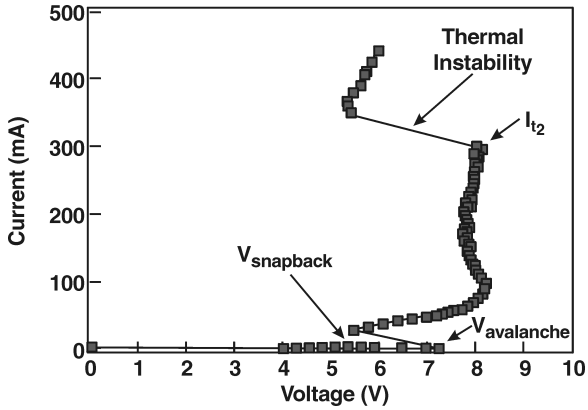

Figure 8. TLP I-V characteristic highlighting the key transition points.

In this TLP I-V plot, the avalanche voltage, snapback and second breakdown current is observable (Figure 8). These are identified by the transitions into negative resistance regimes observed in the TLP I-V plot. The first negative resistance regime is associated with electrical instability, also known as electrical breakdown or "snapback". The second negative resistance regime is known as thermal or second breakdown.

In the TLP methodology, it is common to plot the leakage values after each applied TLP pulse event. As part of the methodology, the failure criteria are a function of the device, and application. In Figure 9, the emitter-base junction of a silicon germanium bipolar transistor was tested in the reverse biased mode with the collector floating. As the device extends beyond the safe-operating area (SOA), leakage increases are evident. Although this is evident, a large increase in leakage is not evident until the device undergoes avalanche breakdown.

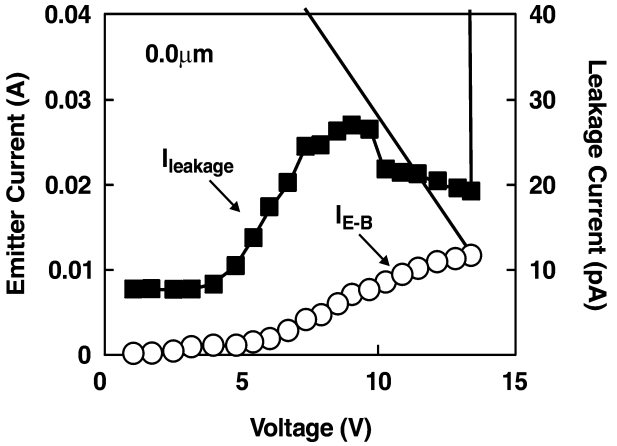

Figure 9. TLP I-V and leakage characteristic of a transistor.

VIII. TLP Methodology Sensitivity to Pulse Waveform Parameter Definition

With the TLP methodology, changes in the parameters can significantly influence the current and voltage characteristics. The current-to-failure and power-to-failure are a strong function of time with the power-to-failure decreasing with increasing time. The dependency of the pulse waveform pulse width is evident in the measurement of the critical current-to-failure, J_{crit}, (e.g. the normalized second breakdown current I_{t2}) of a silicon bipolar junction transistor (BJT) and a SiGe HBT device (Figure 10). As the pulse width increases, J_{crit} decreases. This is anticipated based on electro-thermal physical models, such as the Wunsch-Bell model.

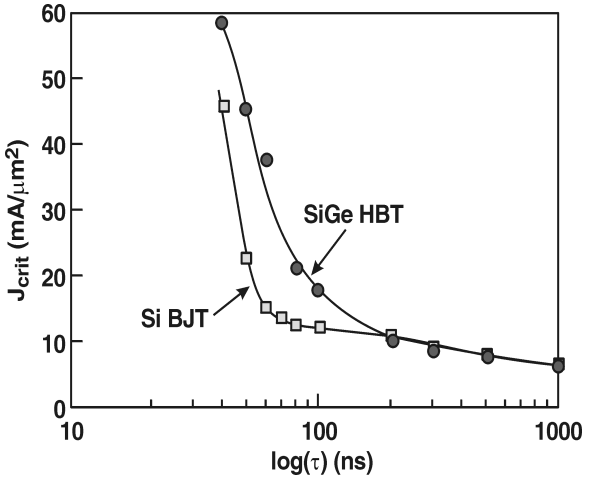

Figure 10. Critical current-to-failure of a Si BJT and SiGe HBT device

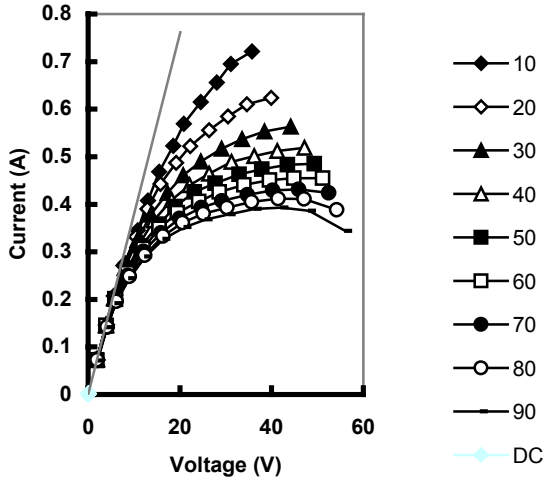

Figure 11. TLP I-V versus measurement window study (for a Copper interconnect).

A. Measurement Window Analysis

The fact that J_{crit} is a function of pulse width is a key reason it is important to establish a fixed value for comparative analysis, dialogue and a specification

Measurement window is also an important parameter in order to insure a procedure for comparative analysis. Placement of the measurement window is important to avoid inaccurate results. In a TLP system whose oscillations and overshoot extends into the pulse, the measurement values extracted for the TLP I-V plot can be altered. Figure 11 shows results from a 450 μm long Cu wire. TLP I-V curves are averages over 9 ns measurement windows centered between 10 and 90ns. For comparison, d.c. I-V measurements on the same structure were made before the TLP curves. The d.c. measurements are shown near the origin and the straight line is a fit to those very low current points. As can be observed, the placement of the measurement window, the width of range over which measurements are taken and the sampling/averaging process can influence the TLP I-V process. In the case of Figure 11 resistance changes with heating are responsible for shifts in the I-V points with the location of the sampling window.

B. TLP-HBM Correlation

It is an interest of the ESD industry to quantify the relationship between the TLP standard method, the human body model (HBM), and machine model (MM) test. A first motivation is be able to provide predictive capability in going from TLP measurement data values to corresponding HBM and/or MM values. HBM and MM tests are the metric for semiconductor quality and reliability used in today's product release process. A second motivation is given that a strong correlation exists between the TLP technique and other ESD model tests, it is possible that in the future TLP wafer and product level testing may replace the need for HBM, and MM testing of products. From early work by ESD researchers, there has been an interest in the relationship between the various models and how they relate to each other.

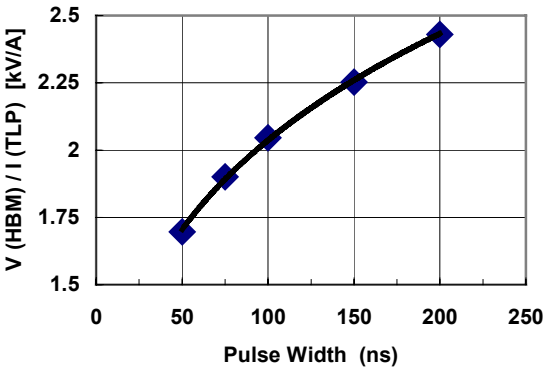

Figure 12. HBM-TLP Correlation as a function of pulse width.

Figure 12 is a comparison of the HBM voltage-to-failure to the TLP current-to-failure of a

semiconductor component as a function of the TLP pulse width. For a 100 ns pulse width, the relationship between the HBM voltage to TLP current is 2 kV (HBM) per A (TLP). This metric is a non-linear and dependent on the pulse width of the TLP test. Hence it is clear that in order to establish a metric between the two methodologies, the pulse waveform must be well defined for the TLP method.

IX. TLP and Derivatives

A primary reason that TLP methodology is of rapidly growing interest is the ability to obtain a pulsed I-V characteristic and identify the first and second breakdown, failure points, leakage history, and resistances. A second reason is that the methodology can be applied on a wafer or product level. A limitation of the TLP methodology is that one obtains only the terminal characteristics of the DUT.

New techniques are being introduced today to both spatial and temporal information to the TLP methodology. A TLP Picosecond Analysis (PICA) tool methodology introduced the ability to provide visualization and animation of the photon emissions on a wafer or chip level after application of a TLP pulse waveform [19]. A second method is the integration of TLP testing and backside laser interferometry [20]. Using optical transient inteferometric mapping techniques, spatial information of the temperature is determined inside the DUT. These methods are an extension of today's practices to provide both the spatial and temporal information within a structure or plurality of structures, which is not obtainable by terminal information.

An extension of this TLP methodology for fast phenomena is known as Very Fast TLP (VF-TLP) [21]. In a standard practice of the VF-TLP method, different system configurations, pulse waveform values and equipment types are required. Although the methodology is distinct, the characteristics and concepts of the TLP SP are related. A key distinction is significantly shorter rise times below 0.25 ns and pulse widths below 5 ns are required

X. Summary

In summary, transmission line pulse (TLP) testing has evolved from the laboratory as a diagnostic tool to a standard practice used for evaluation of electrical components. Today, with the introduction of commercial testers, high quality TLP measurements are being used by semiconductor and component suppliers. TLP measurements are being provided for benchmarking semiconductor devices and technologies, and being provided as a measurement to insure quality and reliability in semiconductor components. The establishment of the TLP standard practice (SP) will provide a means of communication and provide a framework to allow this test methodology to mature into a standard business practice in ESD test and measurement. Today, and in the future, new TLP derivatives and methods will be developed to expand this new methodology. The key question is whether someday in the future whether this rapidly growing TLP method will replace the well-entrenched HBM test method. At this time, it is not clear.

Acknowledgements

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The authors would like to thank and remember the late Hugh Hyatt for his spirit, contributions, insight, and enthusiasm for this new method of testing. He was fundamental voice on introduction of TDR and TDT techniques, and the extension of this TLP methodology to test systems.

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