Voltages Before and After HBM Stress and Their Effect on Dynamically Triggered Power Supply Clamps

R. A. Ashton (1), B.E. Weir (2), G. Weiss (2), T. Meuse (3)
(1) White Mountain Labs, 9831 South 51st St., Phoenix, AZ 85044, USA
Contact: 480-763-0497 X17 e-mail: rashton@whitemountainlabs.com
(2) Agere Systems, 555 Union Blvd. Allentown, PA 18109, USA
(3) Thermo Electron Corporation Lowell, MA 01852, USA

Abstract - HBM and TLP measurements on dynamically triggered CMOS power supply clamps were found to be inconsistent for low leakage clamps. The failures at low HBM voltage were found to be due to a voltage ramp leading up to the HBM pulse which prevented the clamps from turning on.

I. Introduction

Human Body Model (HBM) testing is the most common test for ESD robustness of integrated circuits. This test has proven very successful at predicting the survivability of integrated circuits to ESD events. HBM, with its double exponential current pulse, is not however, the best tool for examining how ESD protection schemes work. This has led to the widespread use of Transmission Line Pulse (TLP) testing for the characterization of ESD protection elements. [1,2] TLP's rectangular pulse makes it a more suitable diagnostic tool. There is usually a good correlation between HBM and TLP results.[3] Unfortunately there are situations in which the results can differ widely.[4] This investigation was launched due to a set of dynamically triggered power supply clamps that were expected to have high HBM failure levels based on circuit simulations and TLP measurements. The HBM results were, however, much lower than predicted. Measurements were made of the voltage during HBM stress to look for clues to the premature device failures. For circuits with low leakage it was found that there could be considerable voltage across a device, both well before the HBM current pulse as well as long after the pulse. Further investigation showed that voltage present just before the pulse could prevent the clamp from turning on, leading to unexpectedly low failure levels for dynamically triggered CMOS power supply clamps.

II. Power Supply Clamps

Dynamically triggered power supply clamps, using a large MOS transistor in normal operation to provide protection, have become very popular in recent years.[5] These clamps have a number of advantages. They can be designed to turn on at low voltage, they do not require special processing, and their operation can be simulated with standard circuit simulation tools.

Several variations of a dynamically triggered power supply clamp were designed and fabricated as test chips in a 0.13 µm CMOS technology. The clamps consist of an RC circuit forming the input of a three stage inverter chain, driving a large nMOS transistor. See Figure 1. The clamp is designed to protect for positive stress of VDD versus VSS and can be a critical element for the protection of inputs and outputs. A positive transient on VDD versus VSS will provide power to the inverter chain and large nFET device. The capacitor will hold node A close to VSS for a time dependent on the RC time constant. As long as node A stays close to VSS the inverter chain will force a high on the gate of the large nMOS transistor, providing a reliable, low resistance, current path for the HBM event. After a time determined by the time constant of the RC circuit, node A will rise to the VDD potential, turning off the clamp.

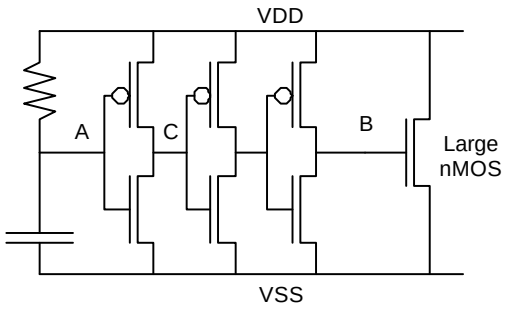

Figure 1 Circuit diagram of dynamically triggered power supply clamps.

TLP measurements of the clamps with 100 ns pulse lengths produced no damage up to 7 A and above, predicting very high HBM robustness for all clamp variations. High HBM passing levels were not obtained on all of the clamps, however. Clamps processed in a high performance version of the technology always passed up to 8000 V HBM stress. Clamps processed with a low leakage version of the technology did not always fare as well. Clamps designed

with a large nMOS with the minimum channel length passed up to 8000 V. Clamps using a large nMOS with longer channel lengths, and therefore lower overall leakage, failed in the 2000 V range. Failure mode analysis revealed a source-drain short in the large nMOS. Test circuits with only the large nMOS hard wired in the off state also showed failure in the 2000 V range, suggesting that the clamps did not turn on during the simulated HBM event. The precise reason for the poor HBM performance of these clamps, however, remained a mystery for some time. The only consistent clue was that low leakage clamps failed at low HBM stress, while high leakage clamps did very well under HBM stress. To help understand what feature of the HBM stress resulted in the poor HBM behavior, voltage measurements were made during HBM stress.

III. Voltage Measurements

The voltage measurements were first performed on Zener diodes, rather than on the power clamps, to provide an easy to understand sample for the development of the measurement technique. A reverse biased Zener diode has a number of useful properties for such a measurement. At low voltage a Zener has high resistance, a diode can be chosen that has a breakdown voltage similar to the breakdown of an integrated circuit, and the diode can carry large amounts of current without damage. Additionally, arbitrary amounts of "device leakage" can be added with a parallel resistor. The Zener diode also provides protection for the voltage probe from high voltage during the HBM event.

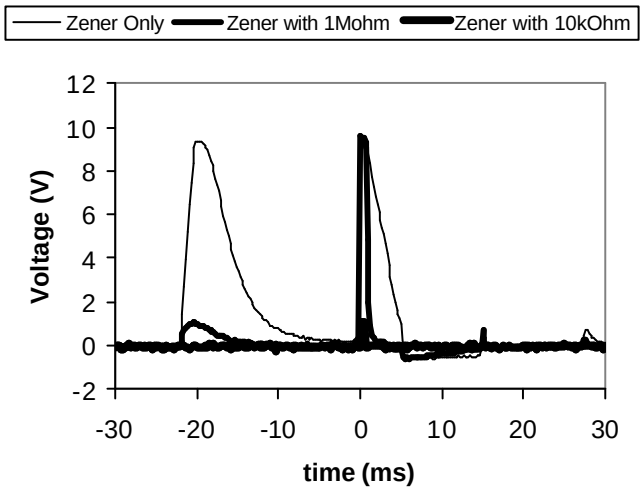

Figure 2 Voltage across Zener diode only with and in parallel with 1MΩ and 10 kΩ resistors for 1000V HBM.

Measurements were made on a Thermo KeyTek Mk2 HBM simulator. The diode was held in a DIP socket. A Tektronix CT-1 probe was attached to the ground side of the Zener diode and connected to channel 1 of a 1 GHz Tektronix TDS680C digitizing oscilloscope. A 10X, 10MΩ, Tektronix P6139A Voltage Probe was attached to the stressed side of the diode and the grounding clip was attached to the grounded side of the diode. The voltage probe was connected to channel 2 of the oscilloscope. The oscilloscope was triggered by the current probe on Channel 1 and the voltages were recorded on Channel 2.

Figure 2 shows voltage data for a 1000 V HBM stress over a very long time period for a 10 V nominal breakdown Zener only, as well as in parallel with a 1 MΩ resistor, and in parallel with a 10 kΩ resistor. The HBM current pulse occurred at time zero, but would be invisible at this time scale

For the Zener only, the measurements show considerable voltages from around 20 ms before the current pulse to about 30 ms after the current pulse. The largest signal occurs before the HBM pulse, peaks near the Zener breakdown voltage, and remains above zero until the HBM pulse at t=0. After the HBM pulse there is another large pulse, lasting about 5 ms, peaking at the Zener breakdown voltage, followed by a period of negative voltage. Finally there is a pair of smaller voltage spikes, one at 15 ms when relays are closed to short all terminals on the device and 15ms later when the relay matrix is reset.

The addition of the 1 MΩ resistor in parallel to the diode greatly reduces the voltage across the diode. The voltage pulse 20 ms before the HBM current pulse is reduced by about an order of magnitude. There is still a large voltage in the period after the current pulse, peaking at the Zener breakdown voltage and lasting approximately 500 µs as well as some very subtle signals just visible Figure 2. With the 10 kΩ resistor there is no pulse 20 ms before the HBM current pulse or well after the pulse. Only a small signal at the time of the HBM current pulse can be seen.

Figure 3 is another measurement of the same Zener diode and resistor combinations at an expanded time scale, but still very long compared to an HBM event. The most obvious feature is the voltage pulse beginning at the time of the HBM current pulse. For the diode only curve the voltage is clamped at the Zener breakdown voltage and remains at that value for a millisecond and then slowly decays over a time of several milliseconds. The voltage with 1 MΩ in parallel with the diode is very similar, with the only major difference being faster voltage decay. With the 10 kΩ resistor in parallel with the diode there is an approximately half a millisecond, 1 V pulse, beginning at the time of the HBM current pulse.

More subtle is the slowly building voltage just before the current pulse at t=0. This is shown in more detail in Figure 4. For the Zener diode the voltage across the device reaches 2 V at the time of the HBM current pulse. The diode with 1

MΩ in parallel has 1 V across it at the time of the current pulse. Only the diode with a 10 kΩ resistor has no voltage leading up to the HBM current pulse. At t=0 there is a spike up to the Zener breakdown voltage followed by a rapid decay to 1 V.

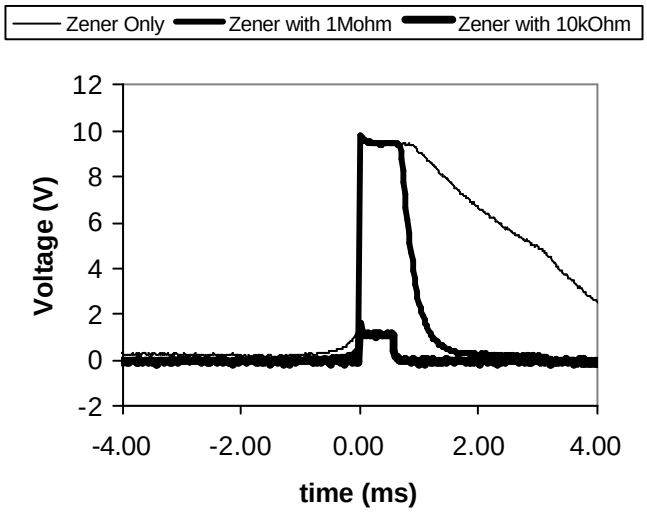

Figure 3 Voltage across Zener diode only and in parallel with 1 MΩ and 10 kΩ resistors for 1000V HBM.

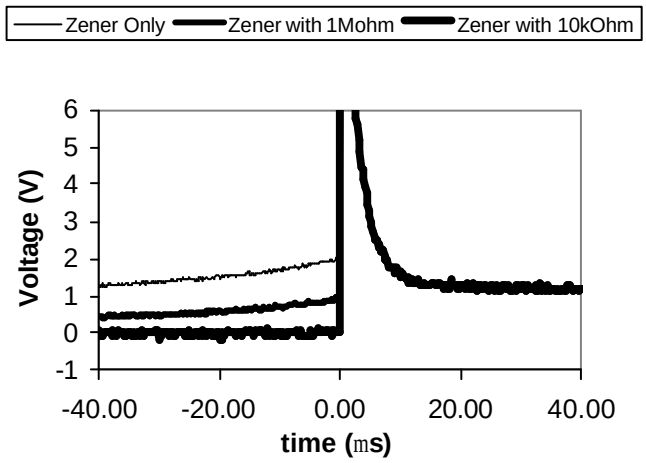

Figure 4 Voltage across Zener diode only and in parallel with 1 MΩ and 10 kΩ resistors for 1000V HBM.

Another factor that could affect the voltage on the device under test is the device capacitance. Measurements with the Zener only and with 100 pF and 1nF in parallel with the Zener are shown in Figure 5. The capacitance has a major effect on the pulse that occurs 20 ms before the HBM current pulse. The capacitance lowers the peak voltage and pushes the peak to later in time. The large capacitance itself can result in a very large voltage offset on the device under test for a very low leakage situation. The effect of capacitance on the voltage ramp leading up to the HBM current pulse can be seen better in Figure 6 where the time scale has been expanded. If the voltage offset caused by the end of the pre-pulse voltage peak is discounted, the voltage ramp leading up to the HBM pulse can be seen in Figure 6. The voltage ramp is seen to be reduced for larger capacitance. In fact there is only a slight rise in voltage leading up to t=0 for the 1 nF case.

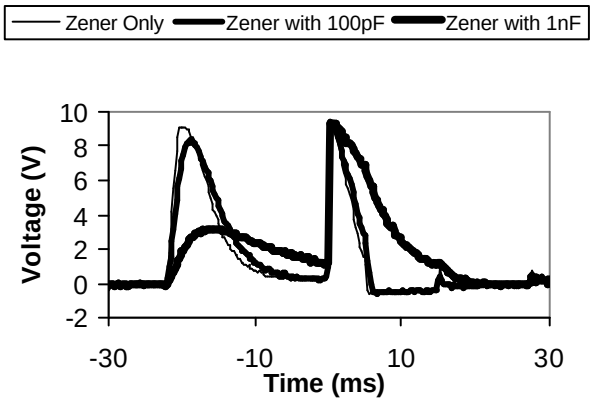

Figure 5 Voltage across Zener diode with and without extra capacitance for 1000V HBM

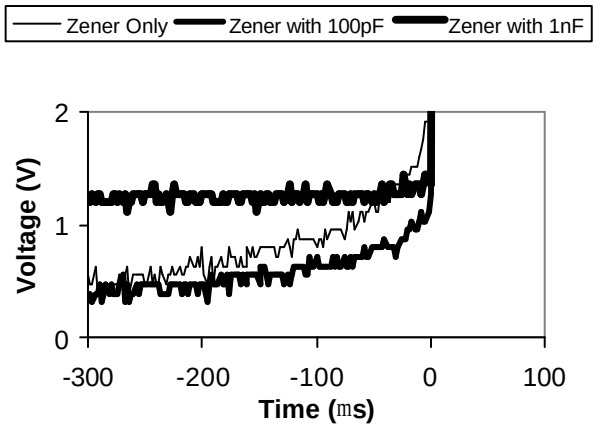

Figure 6 Voltage across Zener diode with and without extra capacitance for 1000V HBM

The origin of the anomalous voltages is still the subject of some speculation. The voltage pulse 20 ms before the HBM current pulse corresponds to the time when the 100 pF HBM capacitor is being charged. Parasitic conduction paths that are part of the machine's switching matrix and other circuitry may allow small currents to charge up the capacitance across the device under test. The voltage drops after the capacitor is charged and the power supply is

disconnected from the 100 pF capacitor. The voltage after the HBM current pulse is due to ionized gas remaining in the HBM simulator relay, providing a current path between the high voltage terminal in the relay and the device under test.[6,7] The voltage build up in the 10 s of microseconds before the HBM current pulse may be the result of ionization in the relay as the relay is closing. This ionization may be enough to provide a high resistance leakage path to charge the device under test but the gas in the relay is not yet able to sustain the low resistance arc that carries the HBM current pulse.

IV. Power Supply Clamp Measurements

The large voltages observed with the Zener diode alone and Zener diode with 1 MΩ resistor suggested that the premature clamp failures could be related to unexpected voltage across the low leakage clamps. Voltage measurements during HBM stress were made on the power supply clamps.

The measurement technique for the power clamps is similar to that used for the diode measurements. The power supply clamps were in 18 pin DIP packages, making handling easy. In order to allow the measurement of the voltage and current and to attach parallel resistors to simulate higher leakage, wires were soldered to the DIP leads, and the wires were inserted into a DIP socket on the HBM simulator. The current probe was placed around the VSS lead. The voltage probe was connected to the VDD lead, with the grounding clip to the VSS lead on the ground side of the current probe. Connections to the oscilloscope were the same as those for the diode measurements. Curve trace measurements were made before and after each HBM pulse to look for device damage.

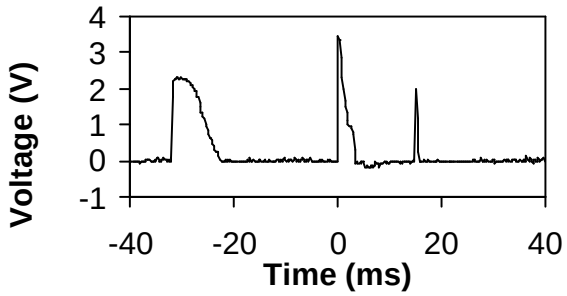

Figure 7 Voltage across a low leakage power clamp for a 1800 V HBM pulse.

The first attempts at measuring voltage across these clamps during an HBM event focused on long voltage pulses, similar to those seen in Figure 2 and Figure 3. A sample measurement is shown in Figure 7 for a low leakage power supply clamp at 1800 V. The device was subsequently damaged with a 2000 V stress. The observed voltages, while significant, do not explain the device failures when compared with known time dependent dielectric breakdown data for the technology's gate oxide.[8] For the dielectric in this technology a pulse in the range of 0.5 ms to 5 ms at 4 V would be required for dielectric breakdown. Dielectric breakdown is also not consistent with the drain to source damage seen during failure analysis.

The presence of the slowly rising voltage before the current pulse in the Zener measurements hinted at a circuit explanation. Voltage measurements during HBM stress were then conducted to look at the time immediately leading up to the HBM current pulse.

Figure 8 shows sample measurements for a low leakage clamp at 500 V and a high leakage clamp at 1000 V. The high leakage clamp shows no voltage build up before the HBM pulse at t=0 and significant voltage only appears after the clamp is expected to have turned off. The buildup in voltage after the clamp turns off is likely due to the trailing voltage pulse as discussed in [6,7]. The low leakage clamp, however, has about half a volt across it at the time of the HBM pulse and shows no extended period of low voltage during the time period after the HBM current stress. This suggests that the power supply clamp never turned on.

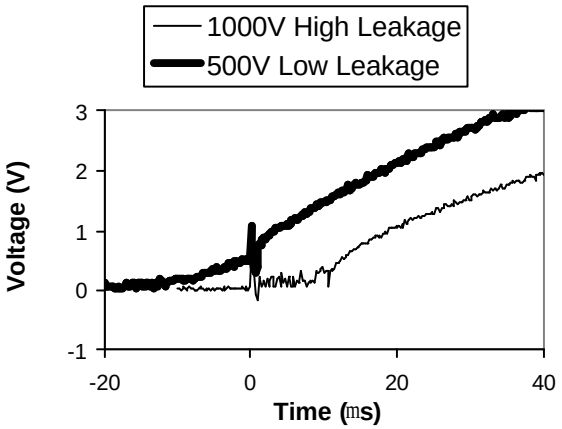

Figure 8 Voltage across power supply clamps during HBM stress, for low leakage clamp at 500 V HBM and for high leakage clamp at 1000 V.

The presence of a voltage across the clamp at the time of the HBM current pulse has major implications for clamp performance. For the dynamic clamp to work properly it is necessary for node C in Figure 1 to be held high for the duration of the HBM current pulse. This can only occur if node A stays below the transition switching voltage for the first inverter. This will be difficult if there is already 1 or 2 volts on node A at the time of the HBM current pulse.

V. Testing of the Theory

A simple experiment was developed to test the theory that the clamp was not turning on because the high resistance

allowed voltage to build up across the clamp before the HBM current pulse. The first step was to do HBM measurements with a 10 KΩ resistor between the VDD and VSS terminals of a low leakage clamp. This resistance is low enough to remove the pre HBM pulse voltage, but large enough that virtually no HBM current can go through the resistor. This will determine if the low leakage version of the power supply clamp can survive an HBM stress if the pre HBM voltage is not present. The resistor can then be removed and the measurements repeated. Voltage was monitored during the measurements to show the lack of, or presence, of the pre HBM voltage.

HBM stress of 500 V to 5000 V was applied to the clamp/resistor combination in 500 V steps.

Figure 9 shows the measured voltage during the HBM stress at 1000, 1500 and 2000 V. No voltage build up is seen before the HBM current pulse at t=0. Note that the after pulse voltage moves out in time for higher HBM voltages and does not show on the time scale of Figure 9. For this reason the higher HBM stress voltage waveforms are not displayed in Figure 9. Figure 10 shows curve traces before the 500 V HBM stress and after 5000 V stress. The presence of the resistor is clearly shown in the curve trace measurements. There is no significant difference in the measurements before and after stress.

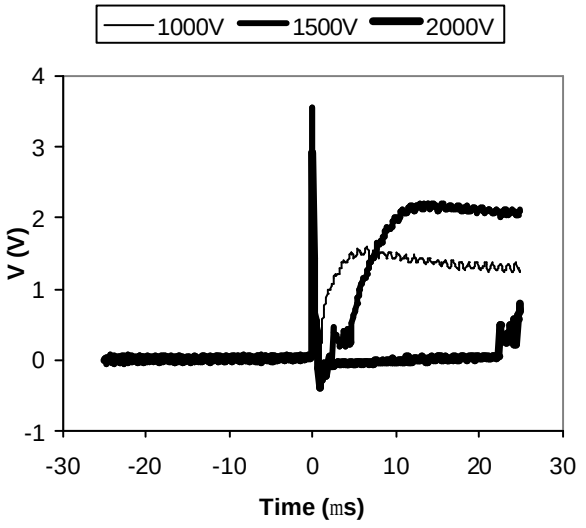

Figure 9 Voltage measurements on dynamically triggered power clamp subject to HBM stress with 10 KΩ resistor.

Figure 11 shows the voltage measurements during HBM stress on the same clamp, without the 10 kΩ resistor for 500, 1000, and 1500 V HBM stress. There is considerable voltage across the device at the time of the HBM current pulse and the buildup of voltage occurs over a time scale much longer than an HBM event or the time constant of the power supply clamp. The 1500 V voltage drops to zero volts at the time of the HBM current pulse, suggesting that the device was damaged at 1500 V HBM stress. Figure 12 shows the curve trace results. The removal of the resistor and the low level of leakage is clearly shown in the before stress and after 1000 V stress measurements. Device failure at 1500 V is clear. Similar results have been seen for two other manufacturers with similar power supply clamp circuits.

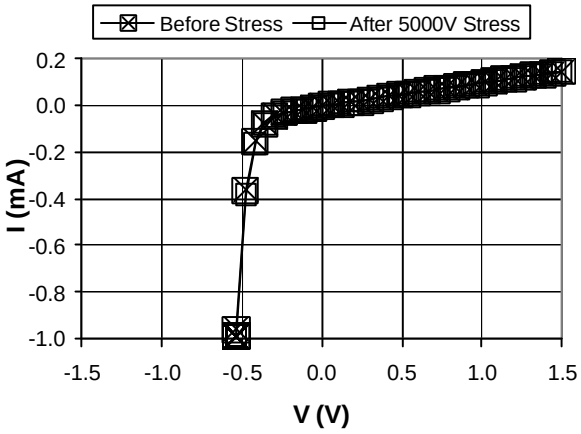

Figure 10 Curve traces of dynamically triggered power clamp with resistor in parallel before and after HBM stress showing no degradation.

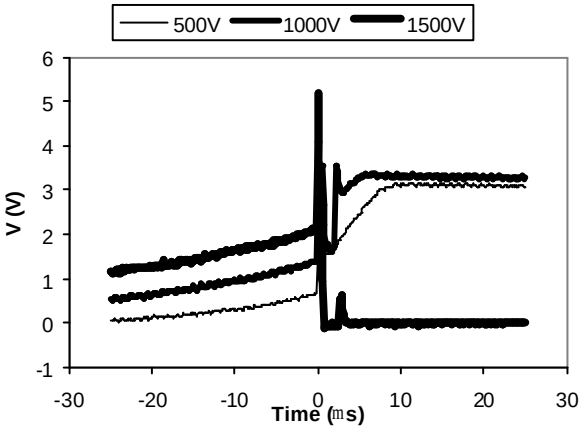

Figure 11 Voltage waveforms on dynamically trigger power clamp without resistor during HBM Stress

VI. HBM Simulators

With the wide variety of voltage signatures seen on the Mk2 simulator it is important to consider if these signals occur only on one HBM simulator. The low failure levels for the low leakage power supply clamps were first observed on a Paragon HBM simulator, and then confirmed

on a Thermo KeyTek ZapMaster as well as the Mk2. We were not able to get voltage measurements on the Paragon but the ZapMaster, with its similar architecture to the Mk2 showed similar voltage behavior on diodes. Measurements were also made on an IMCS 700. The IMCS 700 had very little voltage in the millisecond time period before the HBM pulse and had similar types of voltage after the HBM pulse as the Mk2. In the 10s of micro-seconds leading up to the HBM pulse the IMCS 700 had voltage levels less than those seen on the Mk2, but they are still significant, as shown in Figure 13.

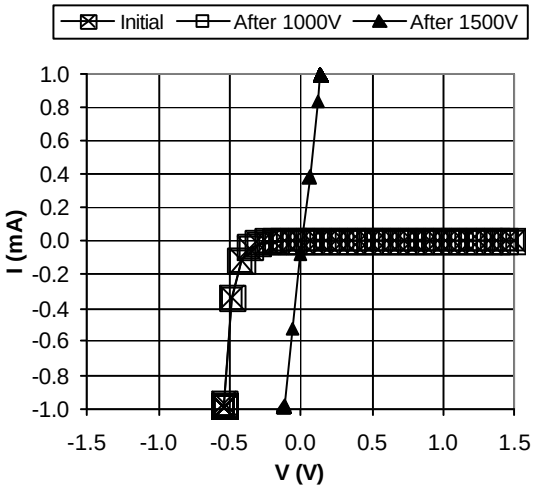

Figure 12 Curve traces of dynamically triggered power clamp without resistor

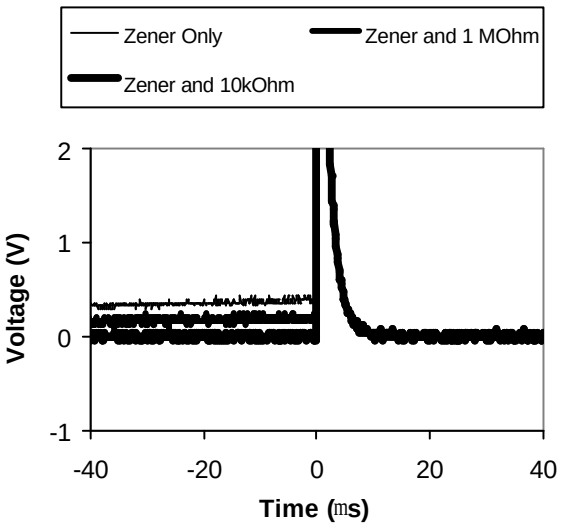

Figure 13 Voltage on IMCS 700 across Zener diode only and in parallel with 1 MΩ and 10 kΩ resistors

The IMCS 700 is a manual HBM simulator with no relay matrix such as those on the Mk2 and ZapMaster. The presence of the voltage just before the HBM current pulse on the IMCS 700 suggests that this voltage may be present at some level on all HBM simulators. HBM stress measurements were also performed on low leakage power supply clamps using the IMCS 700. The failure levels were similar to those on the Mk2. Adding a 10 kΩ resistor in parallel to the clamp resulted in HBM failure levels of approximately 15000 V. This level of failure is very reasonable, since these power supply clamps can handle 100 ns TLP pulses of 7 A without damage.

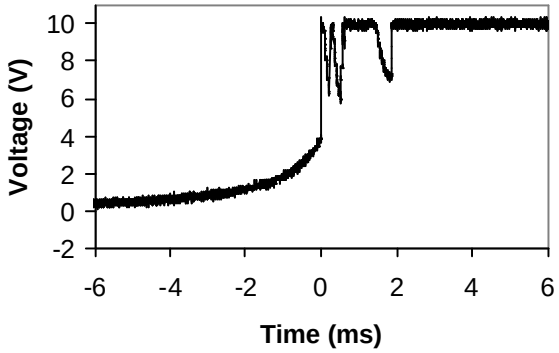

Figure 14 Sample of 2000V Real HBM event

VII. Real HBM

The unexpected voltage ramp leading to the time of the HBM current pulse suggests that the HBM simulators should be fixed to remove the pre-pulse voltage ramp and that the HBM standards should be modified to insure that HBM simulators do not include the voltage ramp. This is only true if a "Real HBM" event, in which a charged person discharges into a high impedance target, does not include such a voltage ramp. Figure 14 shows an example of a real HBM event. This measurement was captured in a way similar to earlier reports on real HBM events.[9] In this case a low capacitance Zener diode was placed on the current sensor and provision was made to measure the voltage across the Zener diode. The oscilloscope was triggered with the current pulse measured by the current sensor and the voltage was captured on a second channel of the oscilloscope.

There is a clear voltage ramp leading up to the time of the HBM current pulse. The time scale of the voltage ramp is about 2 orders of magnitude longer than for the voltage ramps seen on HBM simulators. There is also much more variability in the voltage signals for real HBM events than for an HBM simulator. In many cases the voltage ramp went all the way to the 10 V diode breakdown voltage. There was often considerable structure after the HBM current pulse as seen in Figure 14.

VIII. Conclusions

Measurements of voltage across a device during HBM testing display considerable structure that is very dependant on device leakage. One of the more subtle aspects of the measured voltage is a slow ramp in voltage in the microseconds before the HBM current pulse. The pre-pulse voltage ramp has been shown to have considerable effect on the performance of dynamically triggered power supply clamps. When the clamp and surrounding circuitry have low leakage, the clamp can be prevented from turning on at the time of the HBM current pulse. The first reaction is that the HBM simulators need to be fixed to remove this artifact. Preliminary measurements of the voltage during a real HBM event show the presence of a similar voltage ramp leading up to the HBM current pulse. The presence of the pre-pulse voltage ramp in real HBM events, as well as on more than one HBM simulator, suggest that the voltage ramp is a fundamental feature of ESD discharges to low leakage targets. Removal of the voltage ramp from the HBM simulators is therefore not desirable since it simulates a real world effect. It is desirable that the HBM standards place some bounds on the amount of voltage ramp leading up to the HBM current pulse. Ideally this should be done with reference to real HBM events. This will require real HBM measurements as a function of leakage level across the device being stressed and as a function of the capacitance of the stressed device.

These findings also have a considerable impact on the design of dynamic power supply clamps. It must be understood that under low leakage conditions there may be an essentially DC voltage across the power supply clamps at the time of the HBM current pulse. The amount of the DC voltage can depend on the level of device leakage, the capacitance of the device under test and the details of the HBM simulator. The HBM simulator may affect the size of the voltage ramp depending on the type of relay used to initiate the current pulse, the amount of parasitic resistance in the simulator, as well as the parasitic capacitance of the simulator across the device under test.

IX. Acknowledgement

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