Characterization of Off Chip ESD Protection Devices

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50 Words Abstract – ESD protection devices are placed on circuit boards to protect integrated circuits from ESD stress to systems. There are no generally accepted standards for characterizing the ESD performance of such devices. This article will make recommendations for the proper procedures for characterizing off chip ESD protection devices.

I. Introduction

Electrical systems, from computers to cell phones are tested for ESD robustness according to the IEC 61000-4-2 test standard.[1] ESD protection devices are used on circuit boards to protect sensitive components, such as integrated circuits, from ESD stress to electrical systems. A variety of product types are used including Zener diode-based devices, varistors, and polymer and thick film based protection devices. There are, however, no universally accepted methods for characterizing protection devices for their ability to survive, or provide protection from, system level ESD stress with the IEC 61000-4-2 current waveform. The result is that different manufacturers select different methods, making accurate comparisons difficult. This paper will discuss the properties that ESD protection devices must possess and recommend measurement procedures to allow meaningful comparisons between different protection solutions.

II. Protection Device Properties

ESD protection devices operate by providing a low resistance current path during an ESD event. Protection device properties can be divided into two categories, normal operation and protection operation. In normal operation the protection element must not degrade system performance. At the highest operating voltage leakage must be low to avoid signal degradation and excess power consumption. Capacitance must be low, especially for high speed signals, to prevent signal distortion. The breakdown voltage or trigger voltage must also be above

operation and burn in voltages to avoid turn on of the protection properties during normal operation. The normal operation parameters are usually well characterized on data sheets and will not be discussed further. In protection mode a device must first of all be robust under ESD stress, but that is not sufficient. The device must also maintain low voltage during an ESD event, to prevent damage to sensitive components. Neither ESD robustness, nor the protection properties of protection components are well characterized today for stress with the IEC 61000-4-2 current waveform.
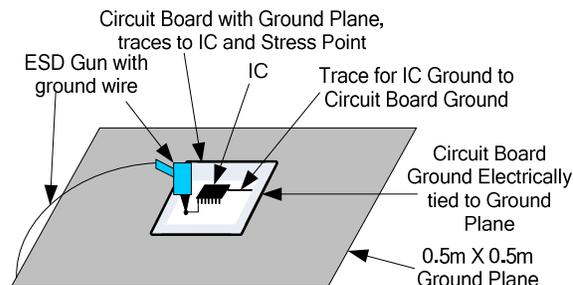

Figure 1 ESD test setup based on IEC 62228.

III. ESD Robustness

Data sheets for protection products typically specify a passing level or voltage per IEC 61000-4-2 [1]. The IEC standard uses a hand-held ESD gun to stress systems from computers to cell phones and is not intended for components. When applied to components the standard does not define component grounding, ESD gun grounding, test fixtures, or waveform verification through the component.

Specialized ESD test standards, such as the IEC 62228 EMC standard for the automotive CAN bus [1], can provide some guidance. The Electrostatic Discharge Association (ESDA) device standards Working Group 5.6 is working on a more comprehensive specification.

The CAN EMC standard defines an ESD test using an IEC 61000-4-2 ESD gun applied to an integrated circuit as shown in Figure 1. The component is mounted on a circuit board in the center of a 0.5 m × 0.5 m ground plane. The need for this ground plane has been investigated by measuring the stress current from an IEC compliant ESD gun doing contact discharge to the center of square aluminum plates of various sizes as shown in Figure 2. A Fischer Custom Communication F-65A current probe was used. The F-65A is a transformer type current probe with a flat frequency response between 100 kHz and 1 GHz. Comparison of F-65A measurements to those performed with the resistive current sensor specified in IEC 61000-4-2 showed virtually identical pulse measurements.
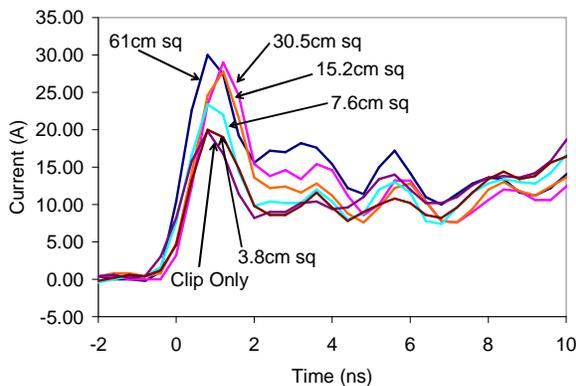

Figure 2 Dependance of initial current pulse on ground plane size

The IEC waveform consists of an initial current pulse with a 0.7 to 1.0 ns rise time, followed by a broader current pulse with lower peak current and can be seen in Figure 3. The ground plane size had little effect on the magnitude of the broad current pulse, but has a significant effect on the size of the initial current spike as shown in Figure 2. Stress to the center of a 0.61 m square ground plane produced the specified 30 A peak current at 8 kV. A 3.8 cm square ground plane, or stress directly to the ESD gun's ground lead, resulted in a peak current of only 20 A. The ground plane is therefore crucial for obtaining the full magnitude of the initial current pulse. The data indicates that the 0.5 m × 0.5 m ground plane in the CAN EMC standard is sufficient. Comparison of

failure levels of a Zener diode-based protection component, however, found no difference between failure levels with and without the ground plane.

The lack of a difference between failure levels with and without a large ground plane can be understood from an evaluation of the energy deposited into the protection element during an ESD stress. Zener diodes fail due to energy dissipation, since they lack the thin oxides which can fail in stress to an integrated circuit. It is therefore important to compare the total energy deposited into the protection element during the stress. Figure 3 shows the captured waveform during stressing of the same diode base protection device with and without a ground plane for a 10 kV IEC stress. The initial current spike is much larger for the test setup with a ground plane than without. During the remainder of the stress pulse with and without ground plane currents have similar values but frequently cross. The difference in current later in pulse will be dominated by factors such as reflections and differences in the inductance of the ESD gun's ground strap from pulse to pulse. To calculate the total power into the protection element requires knowledge of the voltage across the device being tested. As will be seen later it is difficult to measure the voltage across the device during the initial current spike. It was possible however, to calculate the voltage across the device at any current level by using a curve fit to transmission line pulse measurements and the knowledge from VF-TLP measurements that this deice turns on, with no voltage overshoot, in less than 0.2 ns. A calculation of the energy deposited into the device during the first 150 ns of the pulse exhibited less than 1% difference in the energy. This is much too small to be expecting to see differences between the failure level with and without the ground plane.
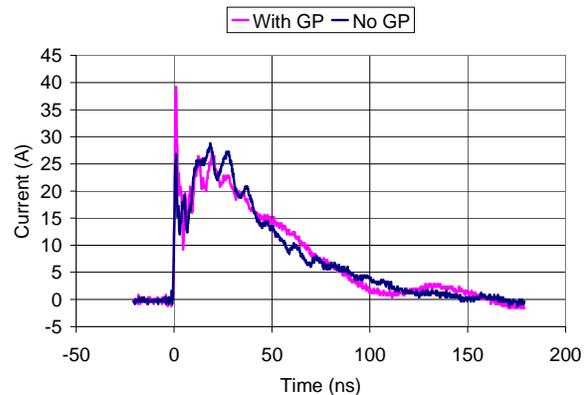

Figure 3 Current waveforms for stress of a diode based protection device with and without a ground plane at 10 kV

IV. Protection Properties

A. Current Practice

There are no standards or even generally accepted procedures for evaluating or specifying protection properties. Methods by some protection device manufacturers include voltage "screen shots" captured during an IEC 61000-4-2 stress, voltage pulse captures during a TLP stress and TLP I-V curves.

A sample screen shot is shown in Figure 4 for an 8kV IEC 61000-4-2 stress.[3] Screen shots show the voltage levels across the protection device during a particular ESD stress and are best when comparing different protection devices. This is shown in Figure 5 where two products are compared, an ON Semiconductor product and a competitor's product. The screen shot quickly demonstrates which product performs superior clamping. It is hard, however, to extract useful parameters such as a clamping voltage or resistivity from screen shots.
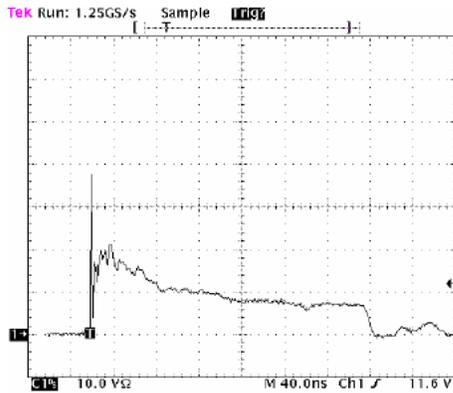

Figure 4 Sample voltage screen shoot of a Zener-based protection device

Transmission Line Pulse (TLP) stress has also been used for characterizing protection elements, especially for polymer and thick film devices. Usually a voltage versus time graph is shown for a 100 ns long TLP pulse at a specified TLP voltage, as represented in Figure 6. These graphics are useful for showing the level of overshoot in polymers and showing relative clamping voltages. These displays are still not sufficient to provide a full description of a protection device's overall performance. Furthermore, the data is often not presented with adequate description of the stress, such as: is the voltage defined into 50 Ω or an open, so that the current during the pulse can be calculated?
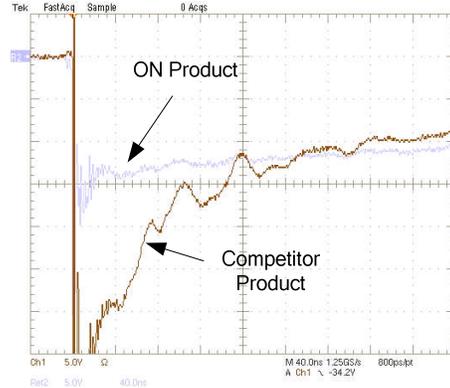

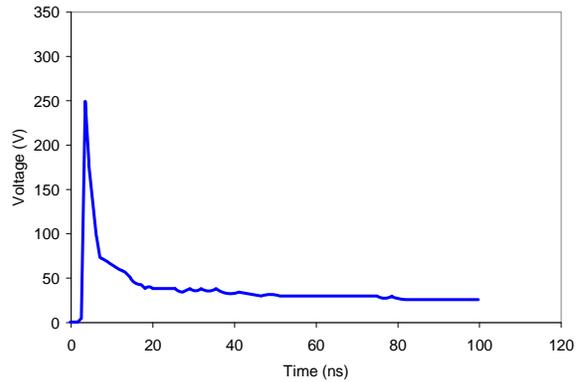Figure 5 Comparison of two diode based protection products with screen shots

Figure 6 Sample TLP result

B. Improved Characterization

Three methods are proposed to provide improved understanding of ESD protection devices. They include the measurement of both current and voltage during an IEC 61000-4-2 stress, 100ns TLP, and Very Fast TLP (VF-TLP).

1. I-V from IEC 61000-4-2

Protection device behavior during an IEC 61000-4-2 stress can be characterized if both the current through the device and voltage across the device are measured simultaneously. This is similar to the simultaneous measurement of voltage and current during an HBM event as reported by Grund et.al.[4] A schematic is shown in Figure 7. A 0.61 m square ground plane has a small circuit board with an SMA connector mounted at the center. The protection element is mounted between the ground and center pin of the

SMA connector which is connected to one 50 Ω channel of a high speed oscilloscope with appropriate attenuators. An ESD gun is discharged directly to the center pin of the SMA connector. The F-65A current probe, discussed earlier, measures the current exiting the ESD gun. The measured current is corrected for current flowing through the voltage measurement channel.
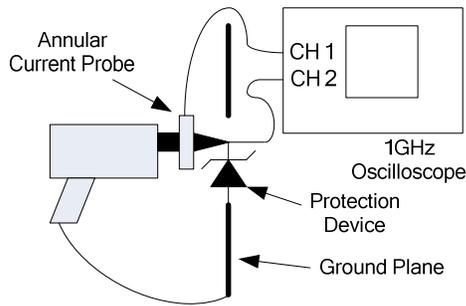

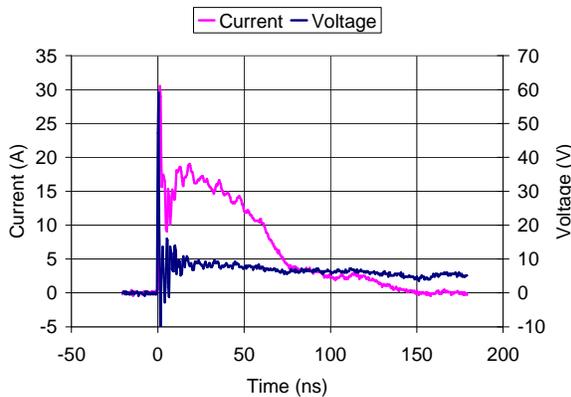Figure 7 Schematic for capturing Voltage and Current during an IEC 61000-4-2 stress

Figure 8 Simultanious measurement of voltage and current during an 8000V IEC 61000-4-2 stress on a Zener-based protection device

Figure 8 shows the simultaneous measurement of voltage and current of a Zener-based protection device. This shows how the protection element quickly holds the voltage under 15 V. An IV curve can be created by plotting the same current and voltage data, time point by time point, as in Figure 9. The data points at the very beginning of the IEC current pulse are dominated by impedance mismatch and an inductive current spike, both of which are unavoidable aspects of the test setup. This creates the outlying data points in Figure 9. After the first several ns of the pulse, the results show a well behaved I-V curve of the reverse breakdown of the Zener diode. This data allows the extraction of resistance and

voltage intercept from the I-V curve. These can be used to predict voltage drops and currents through the device under a variety of stress conditions. The IEC I-V curves also demonstrate the relevance of standard TLP measurements, to be discussed next.
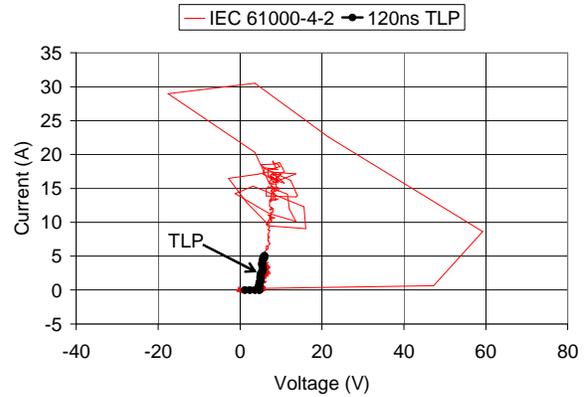

Figure 9 IV curves produced from IEC 61000-4-2 and 120ns TLP on a Zener-based protection device

2. Standard TLP

Standard TLP produces I-V plots similar to those obtained from the simultaneous voltage and current measurement during an IEC 61000-4-2 stress. Figure 9 shows 120 ns TLP data on the same type of Zener-based protection element as the IEC measurement. The advantage of TLP is greater accuracy than possible with the IEC method. This will allow for more accurate measurements of the I-V curve's parameters such as resistance and voltage intercept.
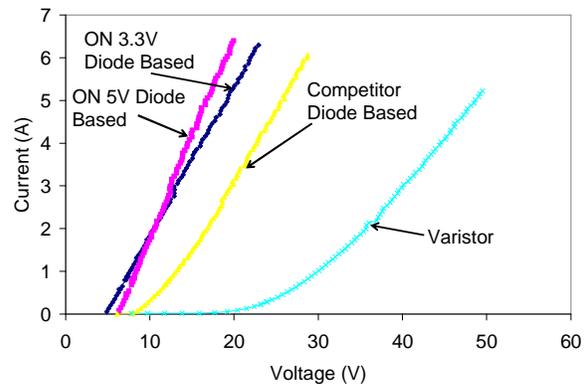

Figure 10 TLP I-V curves of a variety of ESD protection products

Figure 10 compares four different ESD protection products, 3 are diode based and one is a metal oxide varistor (MOV). All of these products are promoted as having IEC Level 4 capability. It is clear that the different products provide radically different abilities to clamp voltage during an ESD event. Even though

the 5 V device's breakdown voltage is higher than the product intended for 3.3 V operation its conductivity in its on state is that much greater than the 3.3 V protection, that the voltage drop is lower at current levels above 2 A. The competitor's diode based protection, intended for 5.0 V operation, has much poorer conductivity at high currents and will provide significantly poorer protection. The MOV has even lower conductivity and would be expected to provide adequate protection only for products which can withstand considerable overvoltage.

3. VF-TLP

VF-TLP extends the benefits of TLP to shorter time domains and is useful for determining the turn on properties of devices. All VF-TLP measurements were made on a Barth Model 4012 CDM-TLP with a 6 GHz oscilloscope. For VF-TLP the test fixture is very important. The SMA circuit board used for the IEC 61000-4-2 voltage and current capture proved an ideal test fixture for time domain reflection (TDR) VF-TLP. VF-TLP pulses with a short replacing the protection element showed a flat voltage response with no inductive spike after the calibration procedure that is integral to the Barth system. Time response will be discussed in greater detail later in this section.

VF-TLP I-V curves explore the time and current domain of the initial current spike in the IEC 61000-4-2 waveform. They may therefore reveal somewhat different characteristics than standard TLP waveforms.

VF-TLP I-V curves are shown in Figure 11 for two bidirectional Zener diode based protection devices. Bidirectional devices behave similar to Zener diodes placed in series, but with opposite polarities. Their breakdown voltage is the sum of a Zener diode breakdown voltage plus a forward bias diode drop in both directions. A unidirectional device by contrast has a Zener diode breakdown voltage in one polarity and a forward bias turn on in the opposite polarity. Figure 11 points out two interesting features. One is that diode A has better clamping characteristics than the competing diode. The other feature is that while both products are bidirectional they have significant asymmetry in their voltage clamping properties. Diode based bidirectional protection products are often built with a combination of surface diodes and diodes built at the bottom of an epitaxial silicon layer. The diodes may have identical breakdown voltages but their conduction properties may be substantially different under a reverse in polarity. Protection devices such as polymers and varistors are inherently bidirectional and do not normally suffer from

asymmetry under polarity reversal. This is a feature that needs to be better understood and characterized on diode based protection datasheets.
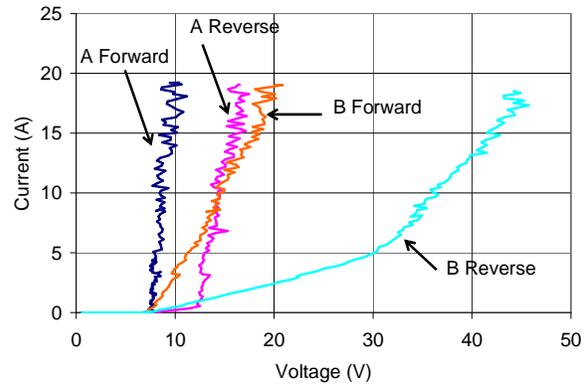

Figure 11 VF-TLP I-V curves of two bidirectional diode based protection devices mesured in both the forward and reverse modes. The pulse length is 5 ns and the averaging window is 2.5 ns in the middle of the pulse.
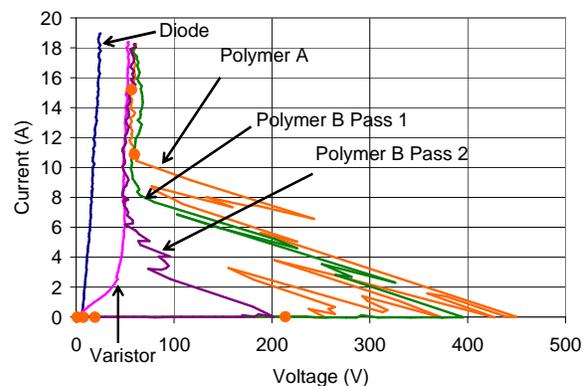

Figure 12 VF-TLP I-V curves comparing diode, varistor and polymer based protecton devices. The data points indicate the VF-TLP pulses on Polymer A included in Figure 19.

Figure 12 compares a diode based protection device with a varistor and two polymer protection devices. One of the polymer devices was measured twice in succession. The diode clearly provides better clamping than the other protection devices. At the highest currents the varistor and polymer products provide similar clamping capability. At lower stress levels the polymer devices display their high trigger voltages and very erratic turn on behavior. Polymer B, which was measured twice in succession, shows that its trigger voltage was cut in half by having been stressed with high currents during the first measurement series. The polymer devices will be discussed further when VF-TLP pulse shapes are examined.

The most important capability of VF-TLP is its ability to look at the turn on properties of devices in the sub ns time domain. The IEC 61000-4-2 waveform's initial peak has a 0.7 to 1.0 ns rise time and real ESD events can be even faster. The Barth VF-TLP tester has a rise time of 0.1 ns and current and voltage sensors with 30 ps rise times. With a 6 GHz oscilloscope the system can easily determine device properties in the 0.1 to 0.2 ns time frame. The limiting factor becomes the test fixture and the ability to separate test fixture properties from the properties of the device under test.

Figure 13 shows the voltage and current pulse shapes for a 490 V pulse into a short on the SMA test fixture after the standard corrections for system impedance. The stress produces almost a 20 A pulse but there is no visible anomaly in the voltage waveform during the pulse. The results are the same for all pulse voltages. It is therefore reasonable to assume that all voltage pulse features are properties of the device under test, rather than the test fixture.

The voltage noise in Figure 13 appears large, but it is an unavoidable result of the calculations required to determine the pulse properties at the device under test for a time domain reflection, TDR, VF-TLP system. The voltage and current at the device under test are determined by adding the incident and reflected voltage and current pulses as well as corrections for system impedance. For a low resistance device under test, such as a short, the reflected pulse has a magnitude almost the same as the incident pulse, but of opposite polarity. Adding these two large voltage pulses of approximately equal magnitude (490 V) but opposite sign produces significant noise. Much of the noise is likely digitization error in the oscilloscope.
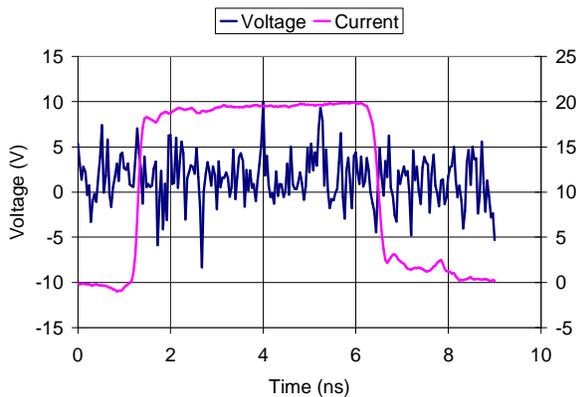

Figure 13 Measured Voltage and Current pulses for a 490 V VF-TLP stress on a short

The potential to characterize device behavior during a current pulse is further demonstrated by the

measuement of a 5 Ω nominal, surface mount resistor, mounted on the test fixture. The current pulse is well behaved but the voltage pulse shows spikes at the beginning and end of the pulse, suggesting inductance in the resistor package. The inductive spikes at the beginning and end of the pulse can be removed, as proposed by Ashton [5], by calculating dI/dt from the measured current and using the inductance as a fitting parameter. The results of such a calculation are shown in Figure 14. The removal of the inductive spikes at the beginning and end of the VF-TLP pulse for the resistor, and subsequent removal from measurements of ESD protection devices, does not imply that the package inductance can be ignored during use of these products. The ability to remove the inductive spikes is instead a confirmation of the nature of the spikes. As will be seen in later measurements, voltage spikes at the beginning of the current pulse are not always caused by inductance.
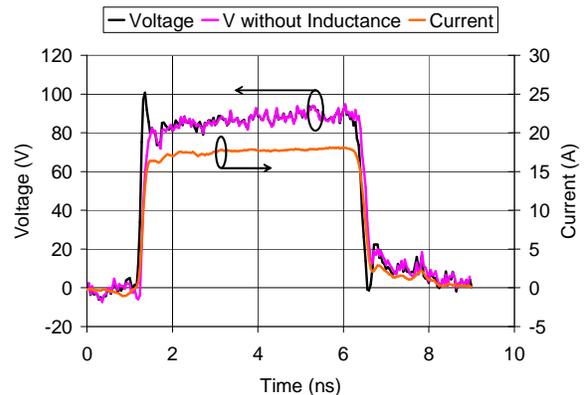

Figure 14 VF-TLP pulse waveforms for a 490 V pule on a 5 Ω surface mount resistor
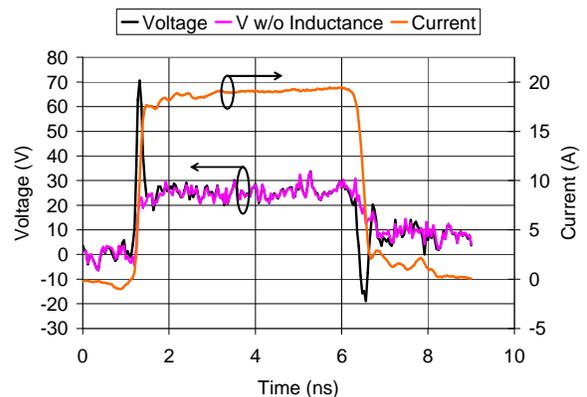

Figure 15 Sample 490 V VF-TLP pulse on Zener-based protection device

Figure 15 shows a 490 V VF-TLP pulse on a 3.3 V, unidirectional Zener-based protection device with a

maximum capacitance of 13 pF. The current rises quickly to over 18 A and reaches a plateau just under 20 A. The voltage clamps to about 10V after an initial voltage spike. The initial positive current spike is mirrored with a negative voltage spike of somewhat reduced magnitude at the end of the pulse. As with the resistor at least some of the initial spike is inductance in the protection device's package. The corrected voltage in Figure 15 assumes a 0.5 nH inductance, very close to the calculated 0.68 nH value for the SOD-923 package. This measurement shows that the turn-on time of the Zener diode, which forms the bases of this protection element, is faster than the measurement capability of the VF-TLP system.

The situation is somewhat different for state of the art Zener diode based protection devices in which the capacitance has been reduced with the use of steering diodes. Figure 16 shows a 490 V VF-TLP pulse across an ON Semiconductor, 5.0 V operating voltage, unidirectional, Zener based protection device with maximum capacitance of 0.9 pF. This device again has voltage spikes at the beginning and end of the current pulse. An inductance correction of 0.3 nH is sufficient to remove the falling edge spike, but it is not sufficient to remove the initial spike. It has been found that this feature is not unique to ON Semiconductor's ultralow capacitance products.
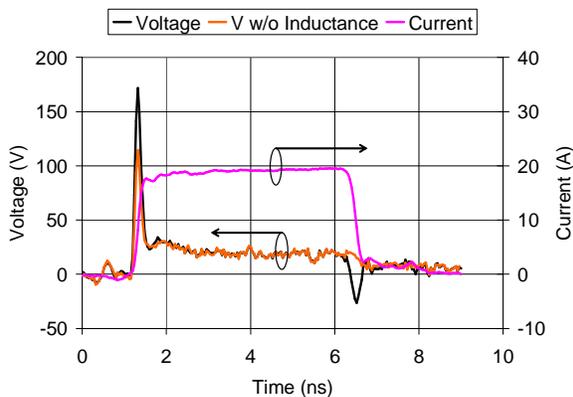

Figure 16 VF-TLP pulse waveforms for an ON Semiconductor unidirectional ultra low capacitance Zener based protection device

Figure 17 shows pulses for a 490 V VF-TLP pulse across a competitor's bidirectional, 0.5 pF capacitance Zener based protection device. This product shows an even larger initial voltage spike that cannot be removed with the 0.7 nH inductance correction which removes the falling edge spike.
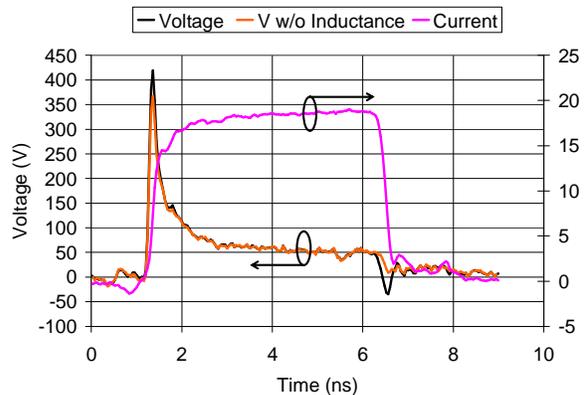

Figure 17 490V VF-TLP pulse waveforms for a competitor's ultra low capacitance Zener based protection device

The voltage spikes at the beginning of a VF-TLP current pulse represent limitations in the ability of an ESD protection device to clamp the voltage of very fast rising current pulses. Spikes due to inductance represent an area where protection manufacturers can improve the clamping ability of products by reducing inductance. The initial voltage spike for ultra low capacitance Zener protection products is not understood, but may represent the intrinsic turn on time of the diodes. System designers concerned with the initial voltage spike may look toward other protection strategies to avoid the initial voltage spikes but there are few options for ultra low capacitance protection. Polymer devices, with their low capacitance, are often considered an attractive protection solution for fast signal lines but they are not perfect solution as will be shown below.
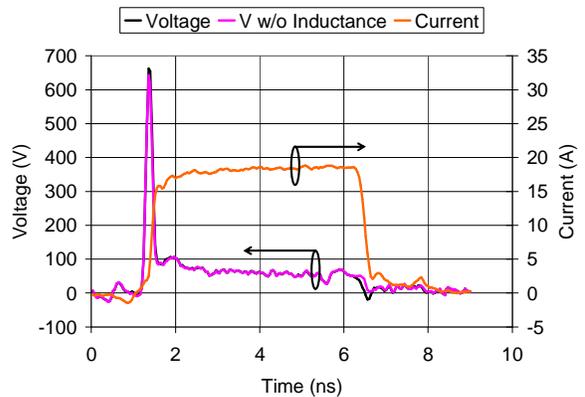

Figure 18 490 V VF-TLP waveforms of a polymer protection device

Figure 18 shows the 490 V VF-TLP pulses for Polymer A in Figure 12. Even with a 0.5 nH inductance correction there is still an over 600 V spike at the leading edge of the current pulse due to

the high turn on voltage of the polymer. At lower pulse voltages polymer devices show additional issues. Figure 19 shows every 20th data point from the data for Polymer A in Figure 12. This data shows that for lower stress conditions the polymer can sustain over 400 V for many ns without turning on. This will expose sensitive components to excessive voltage for long periods. Sensitive components may be able to survive the exposure to over 600 V for less than a ns but they may not be able to survive 400 V for many ns.
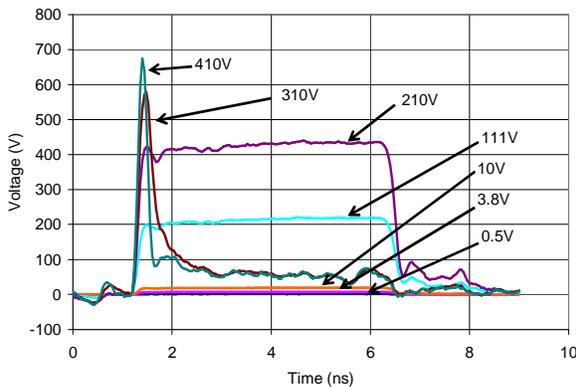

Figure 19 Voltage waveform for every 20th pulse from the data in Figure 12 for Polymer A. The labels refer to the VF-TLP voltage into a 50 Ω load. Figure 12 shows the I-V data points that correspond to the voltage waveforms in this figure.

V. Recommendations

There are currently no generally agreed upon test procedures for evaluating ESD protection components intended for use on circuit boards. Protection components need to be robust under ESD stress, as well as provide a low resistance path when voltages exceed safe levels. Current practice is inadequate in both areas.

A. ESD Robustness Testing

Most manufacturers specify their products based on IEC 61000-4-2, which is not intended for component testing and therefore does not adequately describe the test environment. In the absence of a fully defined standard for determining ESD failure levels for components it is recommended to follow the basic test setup as specified in the CAN EMC standard, IEC 62228.[2] Following this standard will likely make the stress testing similar to more a general component level ESD test specification using the IEC 61000-4-2 waveform that is being developed in ESDA's Working Group 5.6. The basic test setup is shown in Figure 1. The protection device being stressed should be affixed to a circuit board with a large ground plane and short leads between the stress point and the protection device and from the protection device to the circuit board ground. The circuit board should be mounted in the center of a ground plane that is at least 0.5 m square.

Stress to the device should be done with contact discharge only, following the IEC 61000-4-2 procedure of 10 stresses for each polarity and voltage level. All expected current carrying paths should be stressed.

As discussed in Section III, including the ground plane will result in a current waveform that more closely matches the IEC 61000-4-2 current waveform, especially in terms of the initial current spike. For the diode protection product whose failure level was studied the presence of the ground plane was not found to be important, but that is not known to be true for all protection products. For example, polymer devices, with their high trigger voltages, may be aided in their turn on by the initial current spike.

B. Clamping Characterization

Evaluating the clamping properties of protection devices requires the introduction of new techniques. Screen shot voltage capture, as illustrated in Figure 4 and Figure 5 gives a limited insight into a protection device's clamping capabilities. I-V curves at the current levels and time scales of ESD events provide significant insight into a device's protection properties, and should be included on datasheets. Three methods for producing I-V curves for protection devices have been presented here and each has its advantages.

Simultaneous capture of voltage and current during an IEC 61000-4-2 stress has two advantages. ESD guns are readily available which go to 30 kV. At this voltage current in excess of 50 A can be created after the initial current spike. The most widely available TLP and VF-TLP systems do not deliver such high current levels. The equipment for this measurement is also relatively inexpensive. There are two disadvantages. The measurements tend to be noisy and the first few ns of the stress cannot be observed due to measurement issues. (The inability to obtain useful information out of the first few ns helps to keep equipment costs down since a high speed oscilloscope is not needed.)

I-V curves from standard 100 ns TLP will provide much higher quality I-V curves than the simultaneous capture of current and voltage during an IEC stress, or from VF-TLP. Parameters, to be discussed below,

extracted from the TLP I-V curve will therefore be of the highest quality available. A disadvantage of standard TLP is that most systems are limited to 10 or 20 A, significantly below the current levels often available from ESD guns. It is often not possible to bring an ESD protection device to destruction with a TLP system. VF-TLP systems often go to higher currents than standard TLP, but the total energy delivered from a VF-TLP system is even more limited than that available from standard TLP.

The primary use of VF-TLP is to examine the turn on properties of protection devices. The measurements in Section IV.B.3 show the wealth of information that can be determined from VF-TLP measurements of the turn on behavior. The measurements can separate out the behavior of the protection element from inductance in the package. These measurements showed that modern ultra low capacitance diode based protection elements have an initial voltage overshoot that is not present in more traditional diode protection elements. The overshoot for the ultra low capacitance diode products is, however, still much less than observed with the polymer based protection elements.

It would be attractive if a small set of parameters could be defined that would allow direct comparison of different types of protection products. Products such as the two ON Semiconductor diodes in Figure 10 could be easily described by a breakdown voltage and the dynamic resistance of the I-V curve. Other products such as the varistor or the competing diode based product are not well represented by a simple linear fit of the I-V curve. The most desirable characterization is a Spice model file based on the above measurements. This model file could then be used in circuit simulations to predict the voltage across sensitive circuits during and ESD event.

VI. Conclusions

System level ESD protection products are increasingly required by customers in the automotive, medical and mobile markets. ESD protection products have been shown to vary considerably in their protection properties. In order to get comparable and reproducible performance metrics from different laboratories, unified test fixtures and methodologies must be established both for the determination of ESD robustness of the protection devices, and for determining their ability to provide protection to sensitive circuit elements. A standardized test fixture has been proposed for the evaluation of the robustness of ESD protection products. Three measurement techniques have been described that will provide insight into the protection properties of ESD protection devices and will aid in the selection of the of ESD protection products for systems. A variety of recommendations have been made for information that should be provided on ESD protection product data sheets to facilitate accurate comparisons between competing products. There remains a need for Spice models and tools that can be used to predict product robustness during system level stress according to the IEC 61000-4-2 standard.

VII. Acknowledgements

VIII. References

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