FCDM Measurements of Small Devices

M. Johnson (1), R. Ashton (2), S. Ward (3)

(1) National Semiconductor Corp. 2900 Semiconductor Drive, Santa Clara, Ca. 95051

tel.: 408-721-3077, fax: 408-721-2323, email: marty.johnson@nsc.com

(2) ON Semiconductor, 5005 East McDowell Road, Phoenix, AZ 85008

(3) Texas Instruments, 12500 TI Blvd., Dallas, TX 75243

Abstract – Peak current measurements using high bandwidth oscilloscopes show that even small packages exhibit high amplitude FCDM currents. The effects of support templates and vacuum holes on the measured FCDM current waveform are discussed and analyzed, along with other challenges of FCDM stressing small footprint devices.

I. Introduction

Field induced Charged Device Model (FCDM) measurement has attracted considerable attention in the last few years. Papers have shown that measurements with high bandwidth oscilloscopes uncover details in the current waveform that differ significantly between different testers that all meet the specifications and can lead to different test results. [1] Some work has shown that the peak current levels saturate for large devices. [2] Other papers have greatly increased our understanding of the FCDM test with detailed theoretical studies of the test system. [3][5][1] There has been little published on the problems of FCDM testing on small devices (defined as 50% the area of the small JEDEC verification module). FCDM testing of small devices is, however, a considerable problem in the semiconductor industry due to the difficulty of testing. They are not easy to hold with vacuum holes and tend to move easily. The current pulses are also very small and FCDM test machines often fail to detect the FCDM event. The above concerns create considerable problems in the operation of ESD test laboratories. There is considerable support for the idea that testing very small devices (defined as 20% the area of the small JEDEC verification module) for FCDM does not make technical sense. In addition to the handling problems discussed above small devices seldom fail FCDM. The popular explanation is that it is peak current that causes FCDM damage and that the peak current for small devices is too small to cause damage. This has led the JEDEC ESD Working group to consider new rules for the testing of small devices and the current authors were asked to investigate FCDM testing of small devices.

This paper presents measurements of small devices with FCDM utilizing a JEDEC compliant CDM tester. [4] Issues addressed are the true nature of small package FCDM stress by measuring with both 1 GHz and 8 GHz oscilloscopes, the viability of using support templates to improve the handling of small devices during testing, the effect of vacuum holes on test results and the use of surrogates (or conversion boards) to facilitate the handling of small devices. This study led to several conclusions. The assumption that peak current becomes extremely small for small devices is untrue. The use of support templates to facilitate testing is justified. Vacuum holes do present a test issue for very small devices. The use of conversion boards to facilitate the handling of very small devices can be useful under some conditions. The findings are supported by circuit simulations of the FCDM test method. Templates and conversion boards are defined in Section VII.

II. Peak Current Variation

During the months of taking the data for this paper, there were concerns that comparing the data over different test times may need a way to normalize the data. To support this idea, data were taken using the JEDEC small verification module every time the packages of interest were tested. The mean peak current for the 1 GHz oscilloscope was 5.83 A with a standard deviation of 0.27 A at 500 V. The mean peak current for the 8 GHz oscilloscope was 7.49 A, with a standard deviation of 0.37 A at 500 V. All data across the nine months of testing was well within the JEDEC

limits for peak current at 1 GHz and there was no long term drift in the data from either oscilloscope as shown in Figure 1.

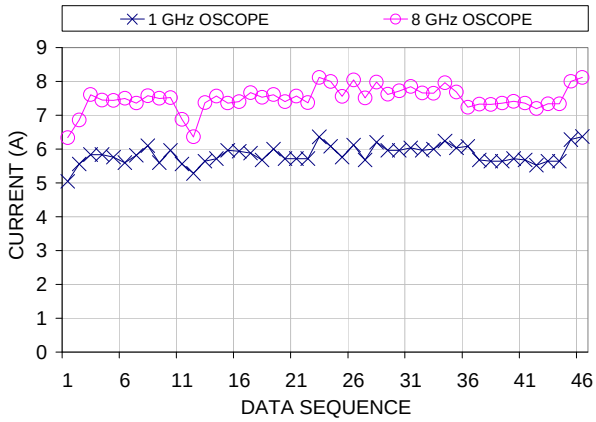

Figure 1. Peak FCDM currents for the JEDEC small module over the time period of the measurements at 500 V.

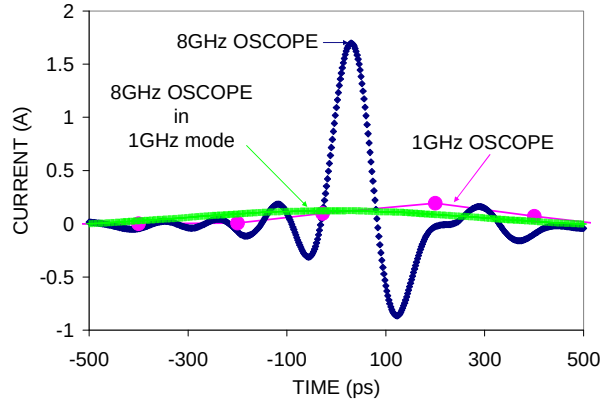

Figure 2. Comparison of FCDM waveforms for 6µSMD (CSP) package with 8 GHz oscilloscope, 8 GHz oscilloscope in 1 GHz mode and 1 GHz oscilloscope at 500 V CDM stress.

III. Oscilloscope Bandwidth

Data showing the effect of oscilloscope bandwidth on the JEDEC CDM waveform [1] has been observed in other work. Those data were taken on the small JEDEC verification modules but there has been little work on samples smaller than the small JEDEC module (area = 8.89 mm^2). The data shown in Figure 2 are from a package considered very small at 1.06 mm x 1.46 mm x 0.6 mm (area = 1.55 mm^2). The graph shows 1 GHz data (Tektronix DPO4104), 8 GHz data (Tektronix DPO70804) and data using the 8 GHz oscilloscope in 1 GHz mode. It can be seen that the 1 GHz oscilloscope misses much of the fine structure of the pulse while the 8 GHz oscilloscope shows a significantly higher peak current. The comparison between the 1 GHz oscilloscope with 5 GS/s and the 8 GHz oscilloscope with 25 GS/s for both the 8 GHz mode and 1 GHz mode illustrates how little data is collected by the 1 GHz oscilloscope. The JEDEC standard uses only information from the 1 GHz oscilloscope to determine the FCDM waveform. Many in the industry believe that small and very small packages do not need testing because the 1 GHz waveform incorrectly measures the peak current.

IV. Peak Current versus Area

The peak current versus package area have been shown in data from others [2] that as package area increases, the peak current begins to saturate, as confirmed by our data in Figure 3 and Figure 4. For large packages there is only a small ratio (1.08) between 8 GHz and 1 GHz data, but for smaller packages the ratio (5.42) becomes very large as shown in Figure 4.

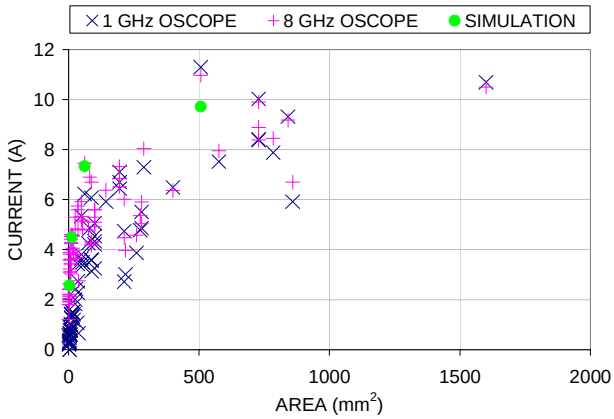

Figure 3. Peak current versus area for all packages tested for this study

The large ratio between the 8 GHz and 1 GHz measurements for small packages is readily understandable if the raw waveforms, as measured with the 8 GHz oscilloscope, are observed as shown in Figure 5. Large packages produce pulses with a width of 1 ns or more, which can be easily resolved by a 1 GHz oscilloscope. Pulses produced by small packages have very narrow pulses, on the order of 0.1 ns. Such pulses are considerably broadened by a 1 GHz oscilloscope but can be easily captured by an 8 GHz oscilloscope.

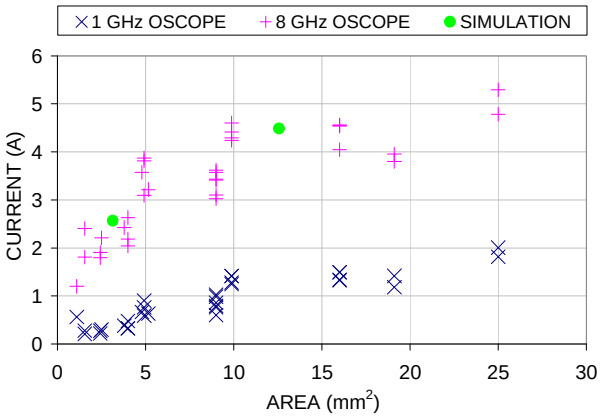

Figure 4. Peak current versus area for small packages (1mm^2 to 25mm^2).

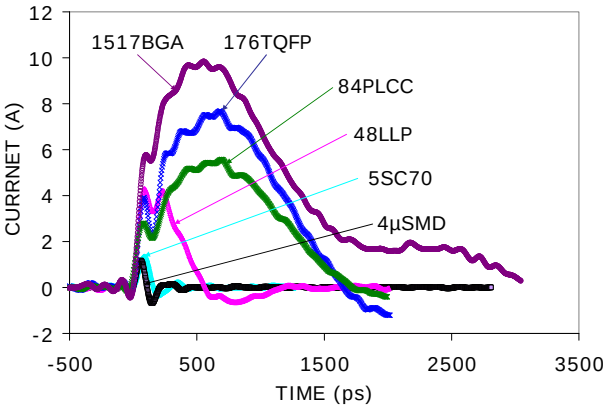

Figure 5. FCDM waveforms for packages of different sizes (V_{CDM}= 500 V & 8 GHz oscilloscope)

Figure 5 shows that the total charge and available energy for large packages is significantly higher than for very small packages. This difference is likely the cause for small devices being able to sustain high voltage FCDM stress. It is not, however, valid to say that small devices survive due to very low peak current. Figure 6 shows an array of some of the parts used in the dataset shown in Figures 3, 4 and 5. The two gold circles are small and large JEDEC calibration modules.

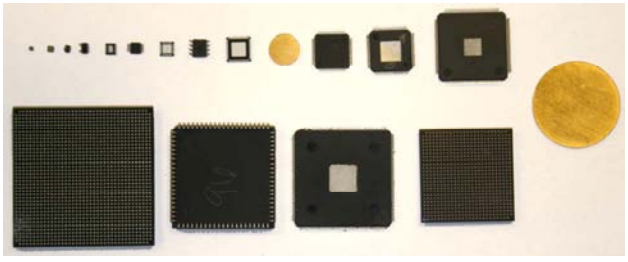

Figure 6. Array of a subset of the devices tested in this study with the small and large JEDEC calibration modules

V. Simulations

Simple circuit simulations shed considerable light on the dependence of FCDM behavior on package size. There have been several models of the FCDM test in the literature. [3][5][1]. The most recent, by Atwood, is the most advanced. Atwood proposed two models, a simple thee capacitor model, similar to earlier models, and a more complete five capacitor model. We believe the three capacitor model shown in Figure 7 is adequate to explain the basics of small package behavior. The three capacitors include the DUT to field plate capacitance, the DUT to ground capacitance and the ground plate to field plate capacitance.

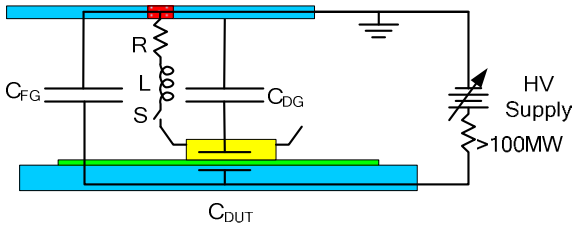

Figure 7. Three capacitor FCDM model

The three capacitor model has been implemented in a circuit simulator. In the model the switch, S, represents the conduction path formed by the arc when the pogo pin approaches the DUT. The switch is considered ideal. The resistor R includes the 1 ohm current sense resistor, resistance in the arc and any resistance added by wave shape forming elements. The inductance, L, includes the inductance of the pogo pin, inductance in the arc and inductance added by wave shape forming elements.

Atwood and Goeau give values for the resistance and inductance but their values are only valid for the ESDA standard not for the JEDEC standard used for these measurements. There is a significant difference between the two standards in terms of the specified wave shape. ESDA specifies a full width at half height of <400 ps for the small, 4 pF, ESDA module and <700 ps for the large 30 pF module. JEDEC specifies a full width at half height of 1 ns ±0.5 ns for both the small, 6.8 pF, and large, 55 pF, JEDEC modules. The wider peak width on the JEDEC standard has forced manufacturers to shape the waveform by adding wave shape forming elements which can include ferrite beads. [1]

Simulations were done for the large and small JEDEC calibration modules and hypothetical calibration modules with 4 mm and 2 mm diameters. All simulations used a module thicknesses of 1.27 mm, 3

mm pogo pin length, 9 nH inductance and 27 ohm resistance. Other values used in the simulations are in Table 1. Capacitor values were based on a parallel plate model, except that a perimeter term was added to the field plate to ground plane capacitance. The calculated value for the DUT to ground capacitor will be particularly inaccurate but this capacitance for the smallest modules is not particularly important. Figure 8 shows the four simulated waveforms along with waveforms captured with an 8 GHz oscilloscope for the large and small JEDEC modules. The peak currents from the simulations are shown Figure 3 and Figure 4.

Table 1 Values used in circuit simulations

Parameter	Large JEDEC	Small JEDEC	4 mm	2 mm
Diameter (mm)	25.4	8.89	4	2
DUT to Field C	55.3 pF	6.78 pF	1.37 pF	0.34 pF
DUT to Ground C	1.5 pF	0.183 pF	0.037 pF	0.009 pF
Field to Ground C	16.1 pF	17.0 pF	17.1 pF	17.2 pF

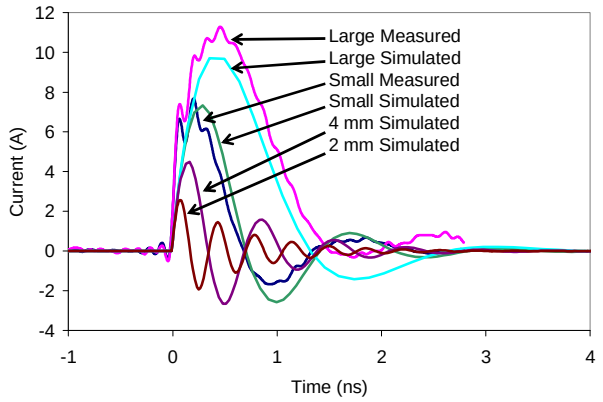

Figure 8. Comparisons of Measured waveforms for the large and small JEDEC modules and simulations

One of the main features of the simulations and measurements is that the peak current does not scale linearly with the capacitance. The simulated peak currents are in good agreement with the high range of the 8 GHz data. It is expected that the simulations should be on the high current side of the measurement spread since the JEDEC style modules represent the high capacitance limit for small FCDM samples of a specific area. The wave shapes for the simulations shown in Figure 8 also follow the same pattern seen for the measured FCDM waveforms in Figure 5. Large area FCDM samples have broad pulse widths while the pulse widths are much narrower for small samples and have a ringing component.

VI. Vacuum Hole Influences

The 1 mm vacuum hole on the RCDM3 tester is comparable in size to the smallest packages tested. This led to the concern that the vacuum hole might affect the peak current. The differences are related to the ratio of the package area to the vacuum hole area (0.785 mm^2) as shown in Figure 9. When the area of the vacuum hole exceeds 18% of the package size the presence of the hole becomes significant.

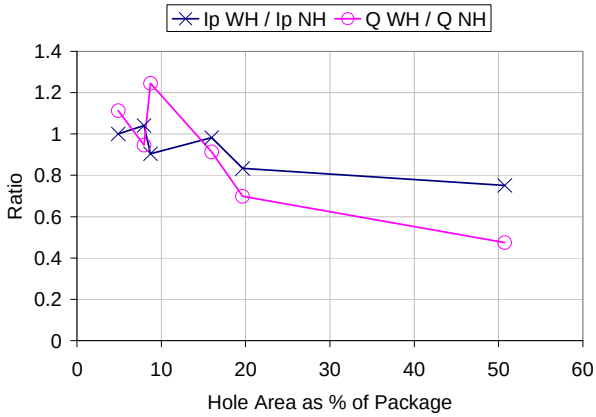

Figure 9. Ratios of peak current and total charge with vacuum hole (WH) and without vacuum hole (NH)

VII. Small Package Handling

CDM testing of products in packages that are very small have been shown to be very difficult. Figure 10 shows a chip scale package without a support template. The mass and spring constant of the pogo pin can easily move the device on any one touch, throwing-off the alignment for subsequent touches. In most cases with very small packages, there are no soft touch settings that will not disturb the position of the package.

The difficulty of testing small packages, coupled with the mistaken view that the peak currents were low, has often resulted in small package parts not being tested. The data presented earlier has clearly shown that the peak currents for small packages are not small. It is therefore necessary to explore techniques allowing efficient testing of small products. Two methods will be shown here and evaluated; the use of support templates to hold the small devices in place and the use of surrogate package or conversion boards to make the device easier to handle.

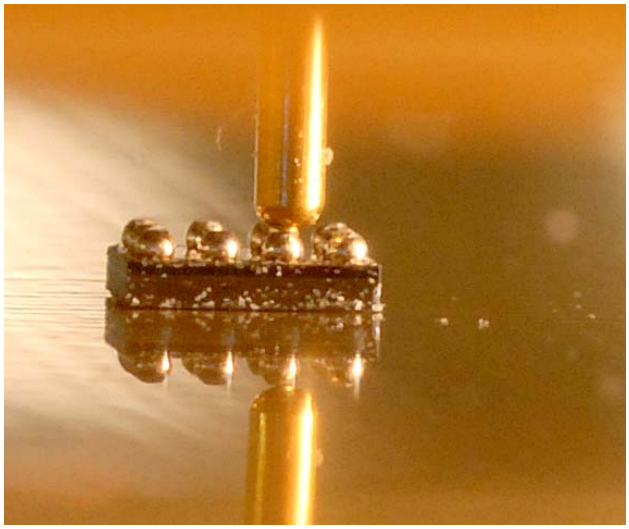

Figure 10. Unconstrained Chip Scale Device in CDM tester (ORION)

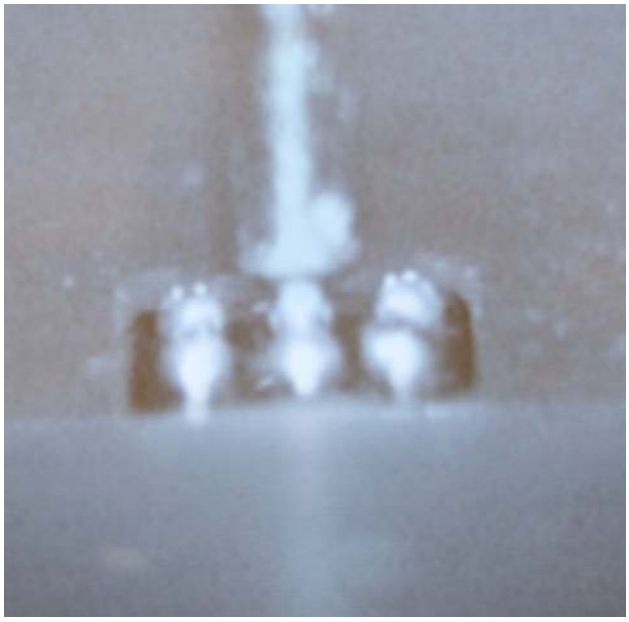

Figure 11. 6µSMD constrained using a support template. (RCDM3)

A template is a thin insulating sheet with a hole just larger than the device being tested. The template is placed on top of the field plate insulator and the device being tested is placed in the hole. The template prevents the device from shifting during FCDM testing. Figure 11 shows a chip scale device with a support template. Support templates are often used to stabilize small packages during FCDM testing. Support templates have evolved from the need to cover unneeded vacuum holes. The initial material suggested by the vendor was thin plastic material. This material was effective at covering the vacuum holes. It was also found to be a stabilizing influence during testing of small parts. This plastic material, however, was difficult to tailor into a small hole for some small and very small packages. The desire for more uniform and easier to construct support templates led to the use of FR-4. The FR-4 can be tailored to match needed thickness and size of the small and very small packages. The FR-4 is significantly more stable and allows solid impact with the device pin or ball. There is always concern, however, that the support template will raise the sample's capacitance. Data in Figure 12 compares a small package (6LLP – 2 mm x 2 mm x 0.75 mm) with and without an FR-4 template. The data indicate that the differences between testing with and without a template are well within the bounds of the variation of the peak current of the RCDM3. The use of support templates does not contribute significantly to the peak current of the device under test or the impedance of the system. Most of these very small packages are nearly impossible to test without the use of support templates.

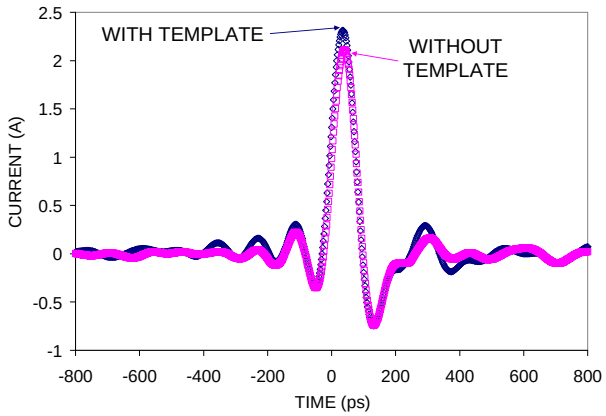

Figure 12. Waveform comparison with and without support template (6LLP at 500 V with 8 GHz oscilloscope)

Another method to test a package is to mount the product (generally a very small package) on small circuit boards that emulated a DIP (Dual-In-line Package). These products were tested using the DIP board (called a conversion board). There were problems with these DIP boards in every phase of the development and changes were necessary. The DIP type devices have always been difficult to test in CDM. This problem was enhanced by the occasional use of parasitic circuit elements on the board. The relative size of the conversion board also made it difficult to see how the data replicated a real life

CDM event for the package. Figure 13 shows a 6µSMD mounted on a conversion board along with a 6µSMD mounted on a surrogate and the 6µSMD.

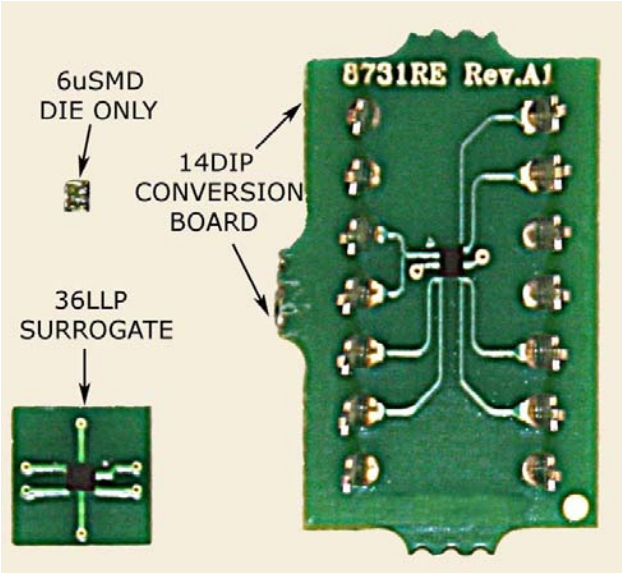

Figure 13. From left to right: 6µSMD (top left) package only; 36LLP surrogate (bottom left) with 6µSMD mounted on it; 14DIP conversion board (right) with 6µSMD mounted on it.

A smaller conversion board emulating a 36 LLP (QFN) was developed. This board gave better responses in product characterization and CDM testing. Figure 14 shows the waveform differences between a chip-scale package (6µSMD), the 6µSMD mounted on a 36 LLP surrogate and the 6µSMD mounted on a DIP conversion board.

The differences indicate a 36 LLP surrogate adds considerably less capacitance to the system than the DIP conversion board and more closely replicates the intent of the test for the product. The net effect of the surrogate is to only slightly intensify the CDM current/charge on the product. The chip scale package (µSMD) shown in Figure 14 is one of the smallest products on the market. As the products increase in size the relative differences in the CDM waveform between the product and the surrogate diminish, as shown in Figure 15.

The inherent testability improves by an order of magnitude with the use of surrogates. Since the CDM tester has limitations in registration at very small pin/ball pitch, the 0.4 mm and 0.5 mm pitches can be tested with the surrogates with significantly less effort and more accuracy.

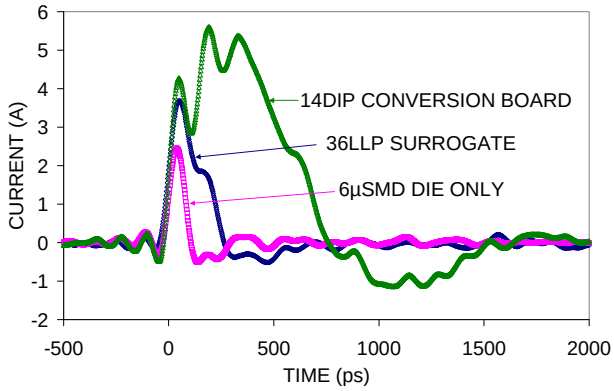

Figure 14. Waveform comparison for chip-scale package (6µSMD) vs 36 LLP (QFN) Surrogate vs 14 DIP Conversion Board at 500V with 8 GHz oscilloscope.

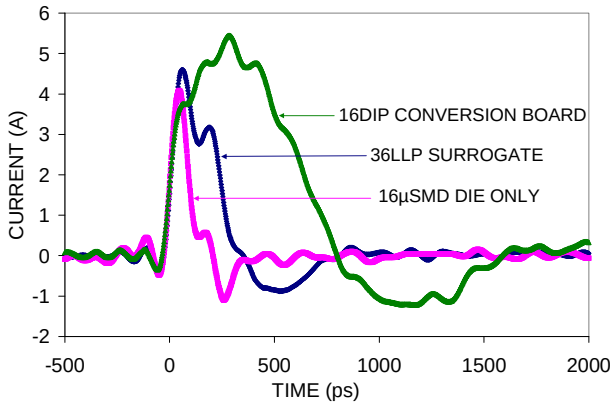

Figure 15. Waveform comparison for chip-scale package (16µSMD) vs 36 LLP (QFN) Surrogate vs 16 DIP Conversion Board at 500V with 8 GHz oscilloscope.

VIII. Conclusions

Measurements with a wide bandwidth oscilloscope show that the CDM peak current, for small packages, does not decrease to negligible levels as previously thought. These results are supported by simple circuit analysis of the FCDM test. The measurements show that the argument to not test small packages due to the low peak current may not be justified. It is possible that small packages may not fail during CDM stress due to the low charge transfer and therefore low energy dissipation. Further research would be needed to justify a proposal to waive CDM testing of small devices. Vacuum holes significantly affect waveform properties when their area exceeds about 18% of the device's area. The use of support templates to provide easier testing of small devices was shown to be a very reasonable procedure. Surrogates can also be used in conjunction with support templates to improve testability with some increase in CDM peak current

and total charge transfer. The tests standards should endorse these approaches for small packages.

IX. Acknowledgements

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X. References

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XI. APPENDIX

The critical dimensions for the packages in Table 2 are listed for reference.

PIN/BALL COUNT PACKAGE TYPE	PACKAGE DIMENSIONS		
	LENGTH (mm)	WIDTH (mm)	AREA (mm^2)
4 µSMD	1.04	1.06	1.10
6 µSMD	1.46	1.06	1.55
5 SC70	2.00	1.25	2.50
6 LLP	2.00	2.00	4.00
8 SOIC	4.90	3.90	19.11
48 LLP	7.00	7.00	49.00
JEDEC SMALL	RADIUS = 8.89		62.07
128 TQFP	20.00	14.00	280.00
JEDEC LARGE	RADIUS = 25.4		506.71
176 TQFP	24.00	24.00	576.00
1517 BGA	40.00	40.00	1600.00

Table 2. Package data for packages described in paper.

The following graphs show the relationship of increasing package area to oscilloscope bandwidth. The five packages show the merging of the 1 GHz and 8 GHz waveforms over the package area spectrum.

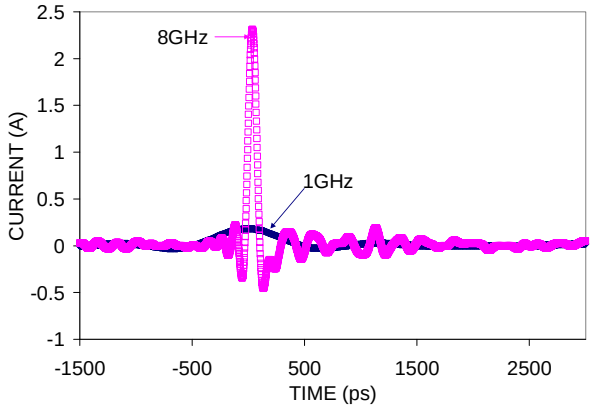

Figure 16. 1 GHz vs 8 GHz oscilloscope data for a 6µSMD

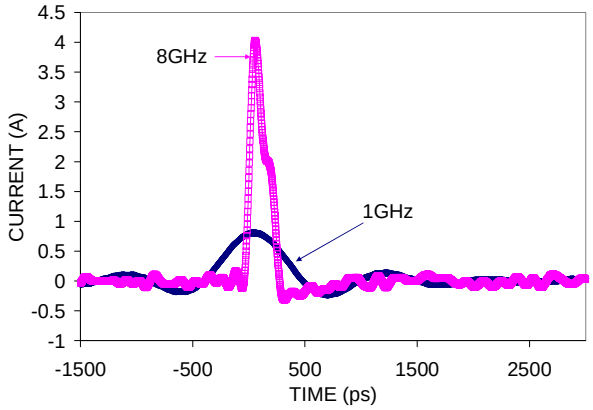

Figure 17. 1 GHz vs 8 GHz oscilloscope data for an 8SOIC

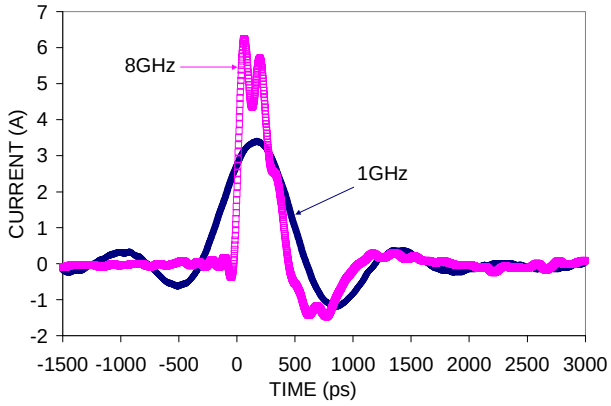

Figure 18. 1 GHz vs 8 GHz oscilloscope data for a 48LLP

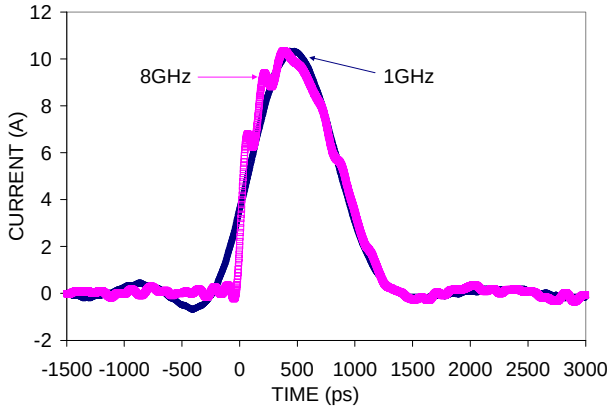

Figure 20. 1 GHz vs 8 GHz oscilloscope data for a 176TQFP

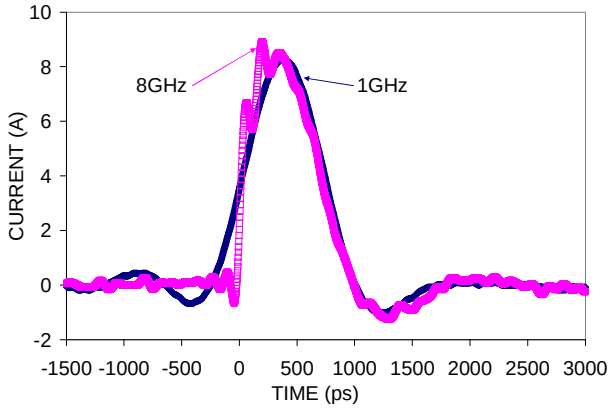

Figure 19. 1 GHz vs 8 GHz oscilloscope data for a 128TQFP