Verification Structures for Transmission Line Pulse Measurements

R.A. Ashton

Agere Systems, 9333 South John Young Parkway, Orlando, Florida, 32819 USA
Phone: 404-371-7531; Fax: 407-371-7577; e-mail: rashton@agere.com

ABSTRACT

Test structures intended for performance verification of transmission line pulse (TLP) systems have been designed and tested. They consist of simple resistors in either copper or silicide clad polysilicon. The copper structures proved unsuitable due to excess heating and melting of any reasonable geometry. The silicide clad polysilicon proved more successful. A simple model of resistive heating accounts for observed non-linearity in the structures under high current stress.

INTRODUCTION

Transmission line pulse (TLP) measurements [1] have become a common tool in the development of on-chip protection from electrostatic discharge (ESD) events. TLP measurements allow the stressing of electrical components at current levels and time scales typical of human body model (HBM) stresses. HBM events have a rise time of 2 to 10 ns, peak currents of up to several A, and a characteristic exponential decay time of 150ns. HBM testing has proven to be a good measure of an electronic component's ability to withstand ESD events in the real word. An HBM, pulse with its rapid rise and exponential fall of current, is not a good diagnostic tool. TLP systems, on the other hand, can test electronic components with a roughly rectangular current or voltage pulse. Typically an I-V curve is measured in which each point in the curve is a single 100ns pulse. An example of such a curve for an n channel transistor is shown in Figure 1. Each point in the curve is an average of the current and voltage over some part of the pulse duration, usually near the end of the pulse.

Verification of the TLP system measurements remains an issue, especially if the measurements are made at wafer level. For TLP systems geared to packaged devices it is possible to use a resistor of known value with a good behavior at high frequency for verification, since a large resistor will not be effected by the high current levels due to the short pulse length. This is not as simple at wafer level where the verification structure should be similar in form to the devices that will be measured by the system. Barth et.al. have proposed the use of a short, a 5 Ω resistor and an open circuit for TLP calibration.[2] The short proposed is a solid gold (10 mil thick) disk. The 5 W resistor would be a chip resistor. The open would be to simply leave the probes unconnected to any sample. This method, while good, does not exactly mimic an on wafer measurement. A better estimate of a short would be to use an on wafer pad of top level metal. This would recreate the exact contact resistance experienced in a real measurement. The use of a chip resistor gives a well controlled resistance value that is likely to be stable even at the high currents of a TLP measurement due to the relatively large size of the resistor compared to an integrated circuit element and the short length of the pulse.

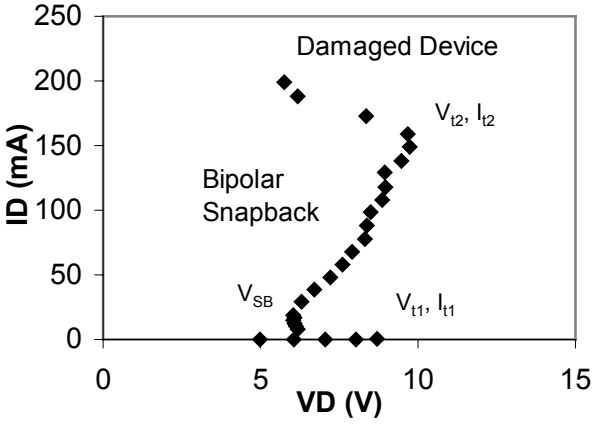

Figure 1 Sample TLP Data for an nMOS transistor. Shows junction breakdown, V_{t1}, biopolar snapback holding voltage V_{SB}, second breakdown point, V_{t2}, and region of device damage.

There are still, however, possible effects which could complicate the transition from the above mentioned "perfect circuit elements" to a real on wafer measurement. These include any unknown properties of the probe pads and contacts down to lower levels that are not examined by the above calibration elements. It would be useful to have a well-understood circuit element that could be placed on wafers in a technology to be studied to insure that measurements made at wafer level are meaningful. This paper will discuss a strategy for making on-wafer verification modules for TLP measurements.

TLP SYSTEMS

Two TLP systems for wafer level measurements were used and are shown in Figure 2. In each system a transmission line of length L, with impedance of 50 Ω, is charged to a voltage. Switching the relay from the charging power supply to a transmission line leading to the wafer produces a voltage pulse with a time length determined by the length of the transmission line, L.

The high impedance version is shown in Figure 2a. During a TLP pulse S_2 is connected to ground and S_3 is open. The termination resistor, R_T, prevents reflection of the incident pulse. The resistor R_S insures that the combined parallel resistance of R_T and the device under test does not deviate substantially from 50 Ω. The voltage V_M across the device under test (DUT) is measured with a high-speed digital oscilloscope and a voltage probe. Current through the device was calculated from the measured voltage and the known

impedances. The high impedance system is best for measuring structures with high resistance and is better suited to detailed measurements around a snapback point. The high impedance system is limited in the amount of current it can deliver to the DUT due to the requirement for high charging voltages to produce high currents and power limitations of the resistor R_T which conducts most of the current from the transmission line.

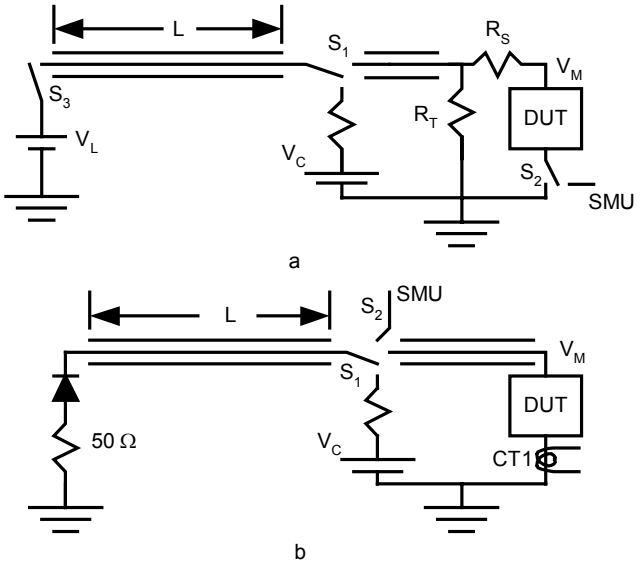

Figure 2 Schematics of high (a) and low (b) impedance TLP systems.

The low impedance TLP system, shown in Figure 2b, is better for high currents but is limited to devices with impedance below 50 Ω. For a DUT with a resistance less than 50 Ω the incident pulse onto the DUT is reflected with a change in polarity. The 50 Ω resistor in series with the diode at the far end of the transmission line provides a non-reflecting termination for pulses whose polarity has been inverted. In the low impedance system the voltage on the DUT is sensed with a voltage probe and the current through the DUT is directly measured with an inductive current sensing Tektronix CT-1 probe.

VERIFICATION STRUCTURES

A verification structure can be any circuit element of known current versus voltage properties in the range of currents and voltages used for real measurements. Experience with characterizing CMOS technologies in the 0.5 to 0.16 μm range of design rules using test structures similar to those described in the SEMATECH test structures for benchmarking CMOS technologies [3,4] indicates the range of values needed. [5,6] Voltages can be as high as 20 V and currents range from tens of mA up to 2 or 3 Amps. This implies the need for verification structures in the range of several ohms to a few hundred ohms. An ideal verification structure is a two-terminal device, since most TLP measurements are done in a two-terminal mode. This is true even when the device under test is not inherently two terminal such as transistors or diffused resistors. Additionally the geometry of the verification structures should be as similar to the devices to be characterized by the TLP system so that there is no confusion in comparing the verification structures with the characterized devices. Ideally the structure would fit between two bond pads of the same type used during routine TLP device characterization. Finally, since device heating during testing is likely due to the high currents involved, it is desirable that the characteristics as a function of temperature be simple and easily modeled. In a basic CMOS technology the only obvious choices are metal and gate resistors.

A set of gate and first level metal structures were designed to test as verification modules. These are shown in Table 1. The structures were built in a 0.12 μm CMOS technology with cobalt silicided polysilicon gate and copper damascene metal layers. The bond pads were covered with aluminum.

The gate modules cover the range of resistances required for the verification structures and fit in the 75 μm separation between the standard test structure bond pads used in the technology. The copper structures only cover the lower end of the desired range and require very long runners, even with a 1 μm wide runner. The copper structures need to bridge several pads making them less convenient, even if they have the necessary electrical properties.

Material	Width (μm)	Length (μm)	Estimated Resistance (Ω)
Gate	60	60	7
Gate	30	60	14
Gate	12	60	35
Gate	6	60	70
Gate	3	60	140
Gate	2	60	210
Gate	1.5	60	280
Gate	0.75	60	560
Metal 1	3	213	7.88
Metal 1	3	453	16.78
Metal 1	1	317	35.19
Metal 1	1	573	63.60

Table 1 Candidate TLP verification modules

MEASUREMENTS

Measurements of the copper structures quickly showed them to be unsuitable. Figure 3 shows current as a function of measured voltage, V_M, for a 3 μm wide runner 213 μm long taken with the low impedance TLP system. The current and voltage are averages between 60 ns and 90 ns of the 100 ns long pulse. The straight line is a fit to DC I-V measurements made at currents at and below 60mA. For the lowest charging voltages the TLP measured I-V shows reasonable agreement with the DC measurements. For higher charging voltages the current saturates at about 0.8 A and then begins to decrease for still higher voltages. The reduction in current at the highest charging voltage is likely the result of copper melting. Higher charging voltages resulted in an open runner. To

measure higher currents would require a wider, and therefore longer, runner to maintain the same low current resistance value. That kind of geometry is unsuitable for a verification structure. Figure 4 is a similar curve for a 60 by 60 μm gate resistor. The results show considerable improvement from the copper example. The current levels are higher than for the copper case and even higher currents could be obtained with a wider resistor. The currents are still highly non-linear. This is presumed to be due to self-heating during the current pulse. The straight line is a fit of DC measurements made with currents below 0.1A. This shows that in the limit of low currents the TLP measurements agree well with the DC values. Better understanding is needed of the high current points.

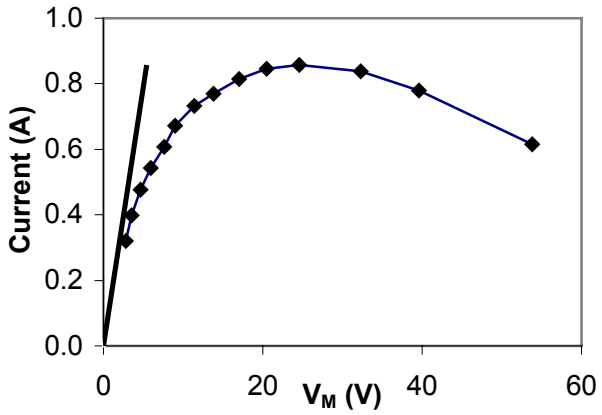

Figure 3 TLP and DC measured I-V curves of copper resistor 213 μm long and 3 μm wide.

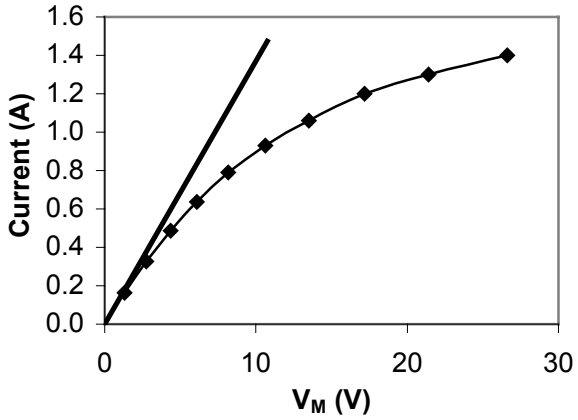

Figure 4 TLP and DC measured I-V curve of a 60 X 60 mm gate resistor.

Figure 5 and Figure 6 show voltage and current versus time measurements similar to those on which Figure 4 is based. The different curves are for different charging voltages. The initial 20 ns of each pulse shows system ringing due to lack of a perfect 50 Ω environment in the home-built TLP system and can be ignored. This data shows how the voltage increases and the current decreases as a function of time, consistent with a model of increased resistance due to resistive heating.

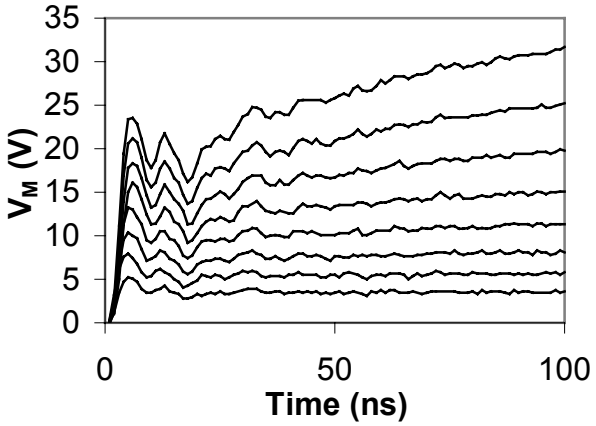

Figure 5 Voltage as a function of time for charging voltages of 20 to 90 V in 10 V steps for a 60 X 60 μm gate structure using low impedece system

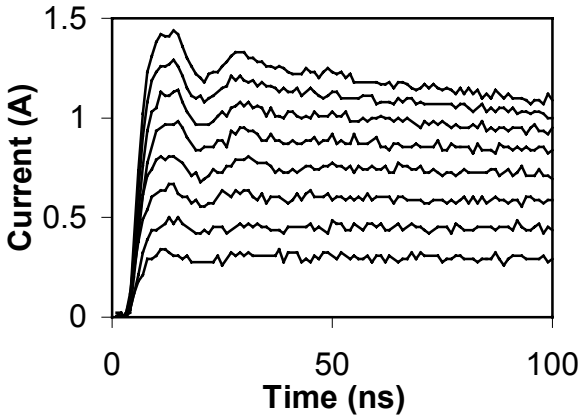

Figure 6 Current as a function of time for charging voltages of 20 to 90 V in 10 V steps for a 60 X 60 μm gate structure using low impedence system.

SELF HEATING MODEL

Before measurements on the verification modules can be used to verify proper system performance, the non-linear behavior must be understood. Figure 7 shows DC equivalent circuits for the high and low impedance TLP systems. A pair of parallel resistors represents the resistances of the cobalt silicide and polysilicon layers of the gate. R_C represents probe contact resistance and any other parasitic resistors in the system. The equivalent circuits show how the current can be calculated from the charging voltage, V_C, and the measured voltage, V_M. The resistance of the parallel combination of silicide and polysilicon resistances is calculated based on the geometry in Figure 8. (In the real structure contact to the gate was of course made at the top surface, not on the ends.)

The room temperature value for the resistance of the polysilicon was estimated from standard I-V measurements of the polysilicon sheet resistance with a silicide block. Temperature coefficients from the standard model file for the polysilicon resistance were used to adjust for higher temperatures. The bulk cobalt silicide resistivity as a function of temperature was used. The silicide thickness was adjusted

at room temperature in the model so that the parallel sheet resistances of the silicide and polysilicon yielded the measured gate sheet resistance.

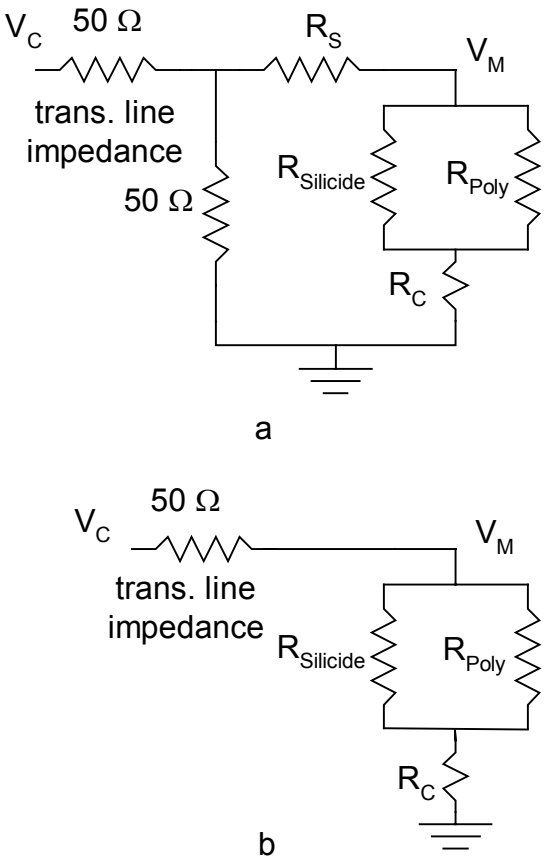

Figure 7 DC equivalent circuits of high and low impendance TLP systems with gate resistance and contact resistance.

The temperature of the gate material was calculated at 1 ns intervals during the 100ns pulse by doing an energy balance between resistive heating and conductive cooling through the oxide, considering the silicon substrate to be a heat sink at room temperature. The thermal mass of the system combined the silicide, polysilicon, and the full block of oxide under the resistor. Considering the full block oxide to be at the same temperature as the conductors is not physically correct but is used to compensate for not including the oxide that totally surrounds the resistor. It would be easy to use the mass of oxide raised to the resistor temperature as a fitting parameter but this was not tried.

Figure 9 and Figure 10 show the same data as in Figure 5 and Figure 6 but include the resistive heating model. The fit of the model is surprisingly good based on the simple nature of the model. The simple model demonstrates that the rising voltage with respect to time for the higher charging voltages and the corresponding decreases in current are the result of resistive heating and not a defect in the TLP system.

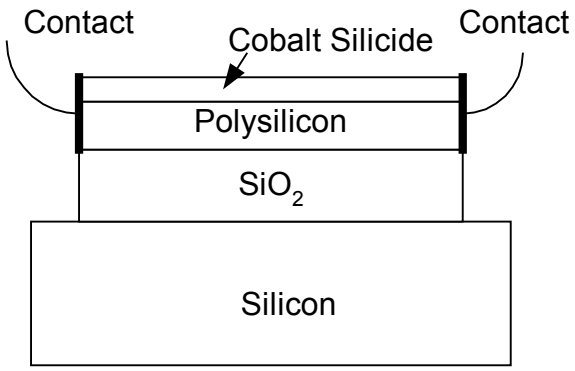

Figure 8 Geometry used for resistance model

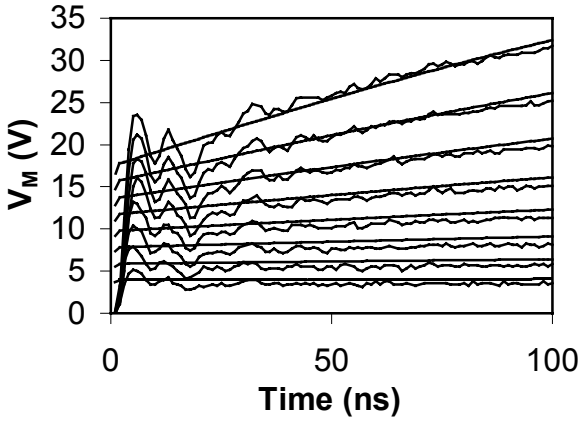

Figure 9 Voltage as a function of time with model calculations added.Same data as Figure 5.

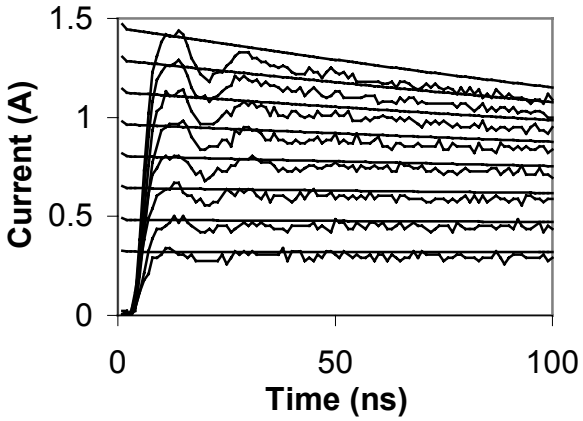

Figure 10 Current as a function of time with model calculations added. Same data as Figure 6.

Measurements have also been done with the high impedance system on a verification structure with a width of 1.5 μm and length of 60 μm. These measurements and the model predictions are shown in Figure 11 and Figure 12. Except for the change in the equivalent circuit, the change in structure geometry and ignoring contact resistance in this high resistance structure all parameters in the model are the same as in used in Figure 9 and Figure 10. The equally good

agreement of the model to the data for this substantially different sized structure is strong support for the validity of the model.

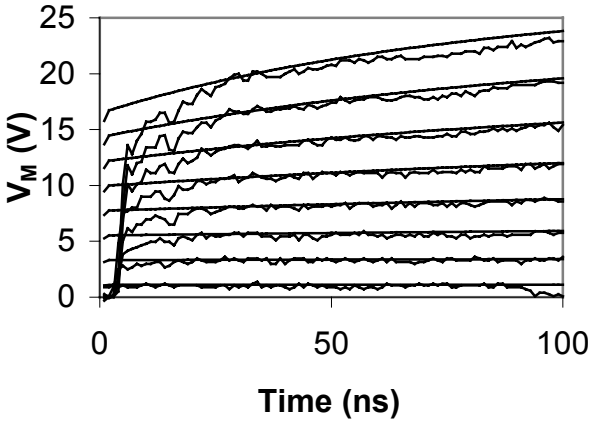

Figure 11 Voltage as a function of time for charging voltages of 5 to 75 V in 10 V steps for a 1.5 X 60 μm gate structure using high impedece system.

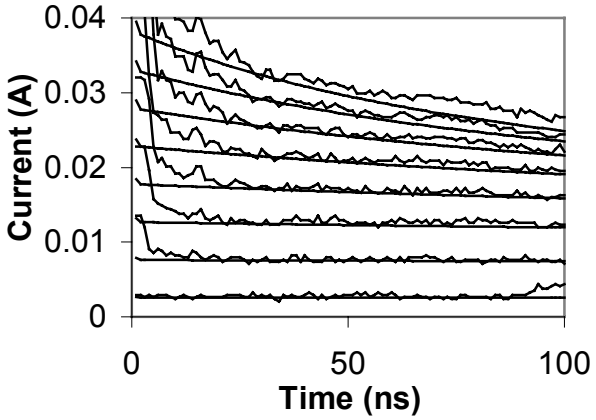

Figure 12 Current as a function of time for charging voltages of 5 to 75 V in 10 V steps for a 1.5 X 60 μm gate structure using high impedece system.

CONCLUSIONS

Test structures proposed for verifying the proper functioning of a TLP system have been fabricated in copper first level metal and in a cobalt silicided polysilicon gate conductor in a 0.12 μm CMOS technology. It has been shown that for reasonable geometries verification structures cannot be made in copper because the metal cannot carry enough current at the required narrow widths. Silicide gate material shows more promise. For reasonable geometries considerably more current can be carried. A simple model shows the non-linear behavior at high currents to be simply resistive heating during the current pulse. A comparison of the measured data with the model shows the TLP system to be free of major problems which would cast doubt on the characterization of more complex devices such as transistors and diodes. To obtain verification modules capable of higher currents the model suggests that wider widths are needed because shorter lengths would increase the resistive heating that causes the non-linearity.

REFERENCES

[1] T.J. Maloney and N. Khurana, "Transmission Line Pulsing Technique for Circuit Modeling of ESD Phenomena", EOS/ESD Symposium Proceedings 1985, pp 114-119.

[2] J.E. Barth, K. Verhaege, L.G. Henry, "TLP Calibration, Correlation, Standards, and New Techniques", IEEE Trans. On Electronics Packaging Manufactruing, Vol. 24, No. 2, April 2001.

[3] SEMATECH Technology Transfer Document "Test Structures for Benchmarking the Electrostatic Discharge (ESD) Robustness of CMOS Technologies", SEMATECH TT 98013452A-TR, May, 1998. http://www.sematech.org/public/docubase/abstract/tech-22.htm.

[4] S.Voldman, W. Anderson, R. Ashton, M. Chaine, C.Duvvury, T.Maloney, E. Worley, "A Strategy for Characterization and Evaluation of ESD Robustness of CMOS Semiconductor Technologies", Electrical Overstress/Electrostatic Discharge Symposium Proceedings, 1999, pp. 212 -224

[5] R.A. Ashton, "Modified Transmission Line Pulse System and Transistor Test Structures for the study of ESD", Proceedings of the 1995 International Conference on Microelectronic Test Structures, pp127-132.

[6]R.A. Ashton and Y. Smooha, "Characterization of a 0.16μm CMOS Technology using SEMATECH ESD Benchmarking Structures" EOS/ESD Symposium Proceedings, 2001.