Electrostatic Test Structures for Transmission Line Pulse and Human Body Model Testing at Wafer Level

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***Abstract*— New two two-pin ESD testers are capable of doing both Transmission Line Pulse (TLP) and Human Body Model (HBM) testing at wafer level. These systems facilitate using test structures to link fundamental circuit element parameters measured with TLP and expected HBM results on final products.**

Keywords—ESD, HBM, TLP

I. INTRODUCTION

Electrostatic discharge (ESD) is a reliability threat to all microelectronic devices. Even when electronic systems are manufactured in an environment designed to reduce the incidence of ESD, all integrated circuits (ICs) must be able to withstand some level of ESD stress. All ICs have specially designed circuits included to protect sensitive parts of the circuit from ESD threats they may experience in manufacture and assembly. Transmission Line Pulse (TLP) has become the standard tool for studying the properties of IC technologies at the current levels (usually up to 10 A) and time domain (several to 100s of ns) of ESD events [1].

Once the final IC has been designed and manufactured it must be tested for ESD robustness to ensure that the ESD design robustness goals have been met. Human Body Model (HBM) is the oldest and most widely performed ESD reliability test for integrated circuits, and is included in almost all integrated circuit qualification plans [2]. TLP testing is often done at wafer level, often on test structures, while most HBM testing is done using matrix based HBM test systems on packaged integrated circuits.

Recently new test systems, utilizing wafer prober technology, have been introduced which can do both TLP and HBM on both packages and wafers. These new testers, often called two-pin testers, have several useful characteristics. One is very low tester parasitics. Capacitive and inductive parasitics, which can be significant in matrix based HBM testers, have been found to create false failures on some integrated circuits. [3,4] A second feature is the ability to do both HBM and TLP at wafer level. Before the development of two-pin testers it was difficult to deliver in specification HBM waveforms to a wafer. The third advantage of the two-pin tester is the ability to measure the current and voltage during an HBM event. The combination of these features in two pin testers improves the usefulness of ESD test structures, providing additional data and options for ESD designers not present when HBM testing was restricted to packaged devices. This paper will discuss the basics of TLP and HBM testing and present TLP and HBM measurements on test structures in a 180 nm high voltage CMOS technology, including DMOS and bipolar structures. The measurements and discussion will demonstrate how TLP and HBM measurement on test structures complement each other and provide more complete information for ESD protection design.

II. HBM AND TLP TESTING

The HBM test is usually represented as a 100 pF capacitor, precharged to a selected voltage, and then discharged through a 1500 ohm resistor to the device under test (DUT), see Fig. 1. The joint JEDEC/ESDA HBM test standard JS-001 [2] defines the stress as a current waveform with requirements through a short and a 500-ohm resistor. The required waveform properties are listed in Table 1.

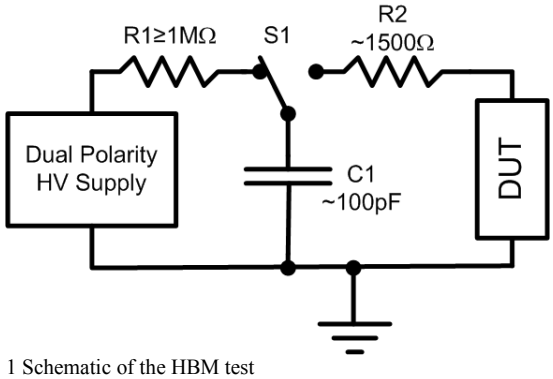

Fig. 1 Schematic of the HBM test

A simplified TLP tester schematic is shown in Fig. 2. A length of coaxial cable is charged to a predetermined voltage and discharged through the device under test. This creates a known amplitude square wave stress pulse whose length, typically 100 ns, as determined by the length of the coax

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cable. Voltage across the device and current through the device are measured during the TLP pulse. By stressing at progressively higher charging voltages, current versus voltage curves can be developed point-by-point. Fig. 3 shows a comparison of the current for a 2000 V HBM pulse with a 100 ns long, 1 A, TLP pulse. The level of stress to a device by induced heating is very similar between the two pulses. TLP has the advantage of creating accurate current versus voltage curves from which one can extract parameters such as breakdown voltage, trigger currents, and dynamic resistance. These parameters are useful for basic understanding as well as circuit modeling.

TABLE 1 Nominal HBM waveform parameters, †500 Ω only specified at 1000 V and 4000 V

Voltage (V)	Ipeak Short (A/kV)	Ipeak 500 Ω (A/kV)	Rise t Short (ns)	Rise t 500 Ω (ns)	Decay t Short (ns)	Ring Current Short
50 to 8000	0.667	0.46†	2 - 10	5 – 25†	150	< 15 % Peak I

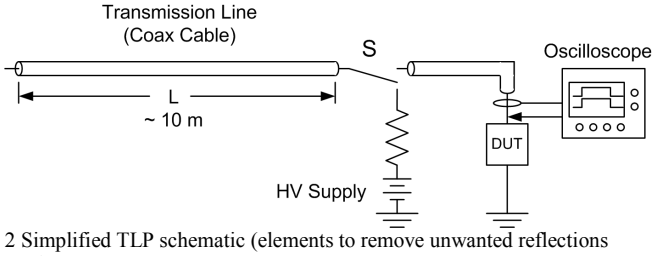

Fig. 2 Simplified TLP schematic (elements to remove unwanted reflections are not shown)

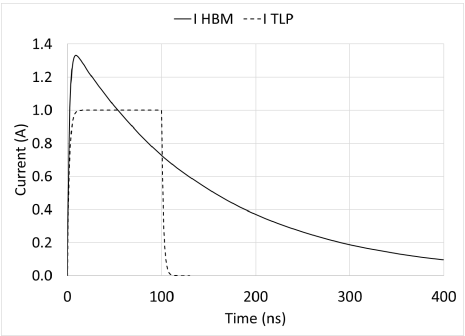

Fig. 3 Comparison of a 2000 VHBM pulse with a 1 A 100 ns long TLP pulse

III. TEST STRUCTURES FOR ESD TESTING

Test structures for ESD can be individual circuit elements, sub circuits containing the elements of an IO buffer, full IO buffers or IO buffers arranged in a full pad ring, but without core circuit elements. The test structures in this paper concentrate on individual circuit elements to show how fundamental ESD parameters, measured with TLP, relate to performance under HBM stress. Examples will be seen where the correlation is good, as well as examples where the difference between TLP and HBM stress become evident and analysis of the voltage and current during HBM events can give valuable information.

Data will be presented on 5 circuit elements and a full protection design, all in a 180 nm high voltage, 25 V, bipolar, CMOS, LDMOS (BCDMOS) technology. The 5 circuit elements consist of a high voltage N-Well diode, a 25 V nLDMOS transistor, 2 SCR designs and a pnp structure.

IV. TEST SYSTEM

All measurements were made on wafer with a Pure Pulse system from Grund Technical Solutions which can perform two-pin testing of wafers and packages with HBM, Machine Model (MM) and TLP stress. The wafer probers are mounted on computer driven micro-manipulators on an automated probe station.

V. RESULTS

A. N-Well Diode:

Diodes are frequently used as part of ESD protection strategies, frequently in forward bias where they are used to steer current away from sensitive elements and toward protection structures. Fig. 4 shows TLP current versus voltage and leakage data for the 40 um wide p-NWELL diode in forward bias. The first observation is that the diode survives 100 ns TLP pulses up to 2 A before leakage develops, revealing junction damage. Fig. 4 also shows a linear fit to the IV curve between 0.1 A and 1 A, yielding a dynamic resistance of 2.2 ohms and a voltage intercept of 1.35 V. These values can be used to predict voltage drops across the diode during an ESD event with currents up to 1 A. For higher currents a more detailed model could be used based on these measurements.

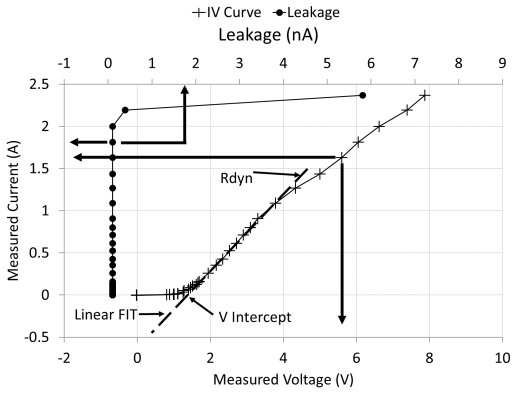

Fig. 4 TLP measurements of a p-NWell diode in forward bias. + marks are TLP IV points. ● marks are leakage measurements made after each TLP pulse. The arrows in this figure, and in the remaining TLP IV measurements, indicate the axes used for plotting each set of points. The y value for the leakage is the TLP pulse current for the pulse proceeding the leakage measurement.

The p-NWell diode was also tested using an HBM stress, without damage, to the system maximum of 4 kV. For many structures it has been found that for each 1 A of 100 ns TLP stress which the structure can survive correlates to 2000 V of HBM robustness. [5] The TLP and HBM measurements on the p-NWell diode are consistent with this correlation.

B. nLDMOS

N channel lateral diffusion transistors serve as drive transistors in high voltage technologies and must be able to survive ESD stress on their own, or be protected by another

element. The grounded gate nLDMOS transistor test structure was measured with both TLP and HBM. The TLP IV curve and leakage measurements are shown in Fig. 5. The TLP IV data shows that the transistor breaks down above 48 V, well above the 25 V working voltage of the technology. On the first TLP pulse above breakdown the device jumps from 20 mA to over 1 A and has high leakage after the 1 A pulse, indicating device damage.

The jump in TLP pulse current from 20 mA to over 1 A is not, however, purely a feature of the nLDMOS device, whether damaged or not. The jump in current is an interaction of the TLP system's 50-ohm source impedance and properties of the nLDMOS device. This is complicated by the fact that nMOS devices often have "snapback" characteristics when the parasitic npn is activated and the voltage can drop to lower values without damage. There may be a section of the nLDMOS's IV curve which can carry current without damage, but is invisible because of the TLP' 50-ohm load line. A potential, but invisible, section of IV curve below the load line in shown in Fig. 5.

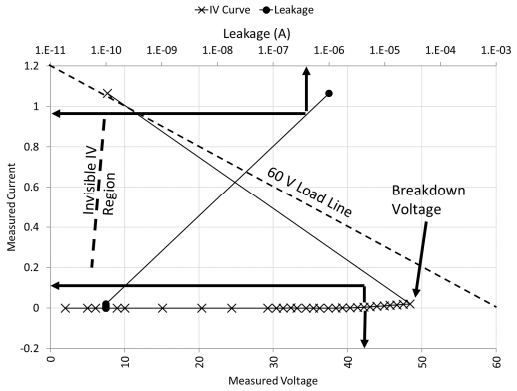

Fig. 5 TLP IV and leakage measurements on the nLDMOS transistor test structure as well as the load line for the final TLP pulse

Each TLP pulse has its own load line. The load lines connect the voltage the TLP system would deliver across an open (zero current), and the current the TLP pulse would deliver through a short (zero voltage). All TLP voltage and current measurements for each pulse must lie on the pulse's load line. The slope of all load lines on the IV is always 1/(50 ohms), but each pulse has a different load line, shifted from the others. The final TLP pulse in Fig. 5 was at 60 V and this load line is shown in the figure. The measured voltage and current for that pulse lies on the load line, as it must. Unfortunately, the TLP current in excess of 1 A damaged the device.

Insight on the potential snapback region can be gained from HBM measurements, since the load line for HBM is determined by the series 1500 ohms resistance, and therefore has a lower slope. Due to the lower slope HBM measurements may be able to "see" the snapback region invisible to TLP. (Note that the load line in HBM is continually changing during each pulse because the HBM pulse is continually changing.)

The HBM data on the nLDMOS showed minor increase in leakage to the transistor at 250 V and 500 V and high leakage after a stress of 750 V. This is well below the usual design targets of 1 or 2 kV HBM. It is therefore necessary that protection structures be added to the IC design to protect the nLDMOS drivers. The TLP data, however, gives the valuable information that the nLDMOS has a breakdown voltage at or above 48 V. The necessary protection device needs to have a trigger voltage below 48 V to protect the nLDMOS transistor, but above the 25 V working voltage for the technology to prevent unintended operation.

Because the two-pin tester measures both voltage and current during each HBM pulse we can look for the presence of a snapback region. Fig. 6 and Fig. 7 show the current and voltage as a function of time for the three HBM pulses. The current looks superficially like the expected exponential decay but drops to zero late in the pulse, rather than exponentially approaching zero as current through a short or resistor would. After an initial voltage spike the voltage drops to below 5 volts before increasing to a higher voltage at the same time as the current drops to zero. This is the snapback region which could not be seen in the TLP data. The increase in voltage late in the pulse is when the current gets too low to sustain the snapback.

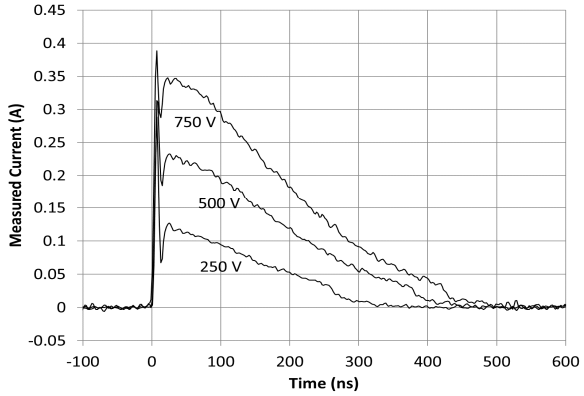

Fig. 6 Current versus time for the three HBM pulse on the nLDMOS

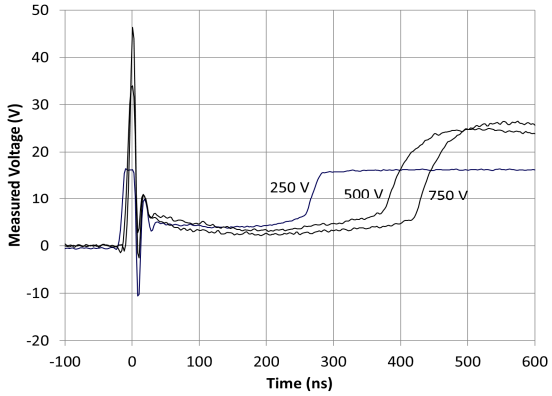

Fig. 7 Voltage versus time for the three HBM pulses on the nLDMOS

It is also possible to construct an IV curve from the HBM data. Fig. 8 shows an IV curve derived from the 750 V HBM pulse. For each 2 ns time interval from 32 ns to 600 ns, a current versus voltage point is plotted, forming an IV point-by-point. This creates an IV curve as the current decays. This

clearly shows the snapback region and how the low voltage state is lost when the current falls below 40 mA.

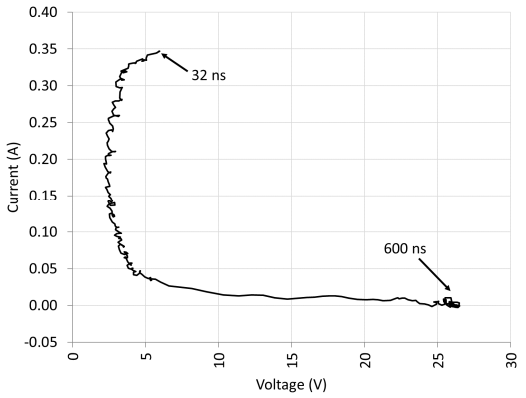

Fig. 8 IV curve of the nLDMOS device derived by plotting current versus voltage time point by time point starting at 32. ns into the pulse and ending at 600 ns

C. SCRs

Silicon Controlled Rectifiers, which consist of an npnp structure, can be very effective ESD protection devices. SCRs can have a high breakdown voltage, but when triggered they snapback to low voltages. With the low snapback voltage SCRs can carry considerable current, while dissipating relatively low power. This makes them very efficient ESD protection structures.

Fig. 9 shows TLP data for SCR Design 1. The device has an initial breakdown of 43 V, deep snapback to below 5 V and carries up to 4 A of current without damage. This predicts 8 kV of HBM robustness, which was is consistent with its passing the maximum 4 kV level of the HBM stress. Protection devices with deep snapback, however, need to be used with caution. There are two issues. Will the device present a latch-up risk during normal operation, and will the protection device turn off prematurely as the HBM current decreases?

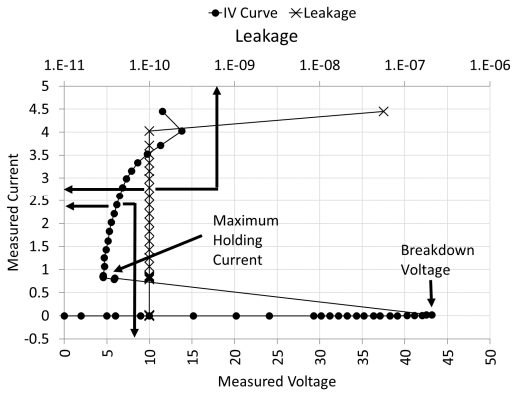

Fig. 9 TLP measurements of SCR Design 1. The device shows deep snapback and a failure at 4 A.

If the holding current for the snapback state is less than what the system power supply can supply there is danger of latch-up or oscillation. The data in Fig. 9 suggests a holding current of about 0.8 A. As discussed in the section on the nLDMOS, the properties of the TLP system can mask part of the snapback region due to the 50-ohm load line. The TLP measurement of 0.8 A for the holding current is therefore a maximum value. The true holding current could be much less. The source impedance of the HBM source is 1500 ohms and can give better insight into the true holding current of the snapback state.

Fig. 10 and Fig. 11 for SCR Design 1 show current and voltage during HBM stress.

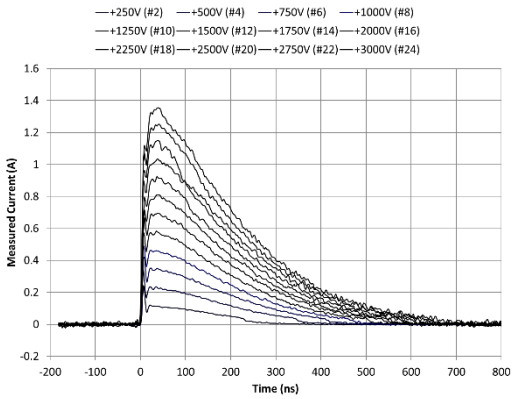

Fig. 10 Current versus time measurements on select HBM pulses for SCR Design 1

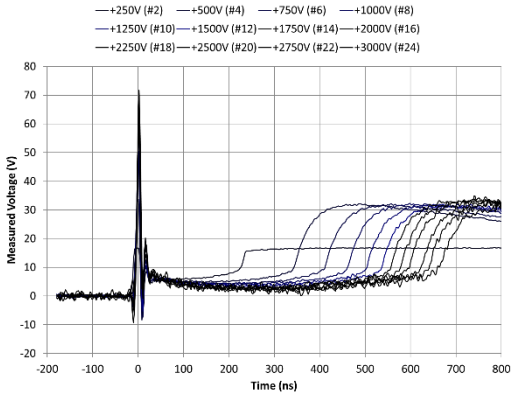

Fig. 11 Voltage versus time measurements on select HBM pulses of Field Oxide Device

Fig. 10 shows the expected HBM current waveforms, except that at some point the current becomes zero, rather than asymptotically approaching zero. Fig. 11 for voltage shows an interesting story. After an initial voltage spike, the SCR turns on, clamped the voltage to below 5 V, as predicted by the TLP curve, Fig. 9. Later in the pulse the voltage rises again, when there is insufficient current to maintain the SCR action, but the HBM 100 pF capacitor still has 30 V remaining from the initial charge. This is consistent with the concern raised above, that at some point the SCR can no longer sustain the low voltage state. Any device being protected by this SCR needs to be able to either survive a relatively long exposure to about 30 V or be able to handle the current from the charge remaining on the 100 pF HBM capacitor. A question remains, what is the holding current for SCR Design 1? Further insight can be found by looking in greater detail at the HBM current waveforms, as shown in Fig. 12. This is the same data as shown in Fig. 10, but with an expanded current axis. At

roughly 38 mA all of the HBM current pulses break from their exponential decay and drop more rapidly to zero current. This drop in current coincides with the increase in voltage seen in the voltage versus time curves in Fig. 11. This suggests that the holding current for the SCR is 38 mA or less.

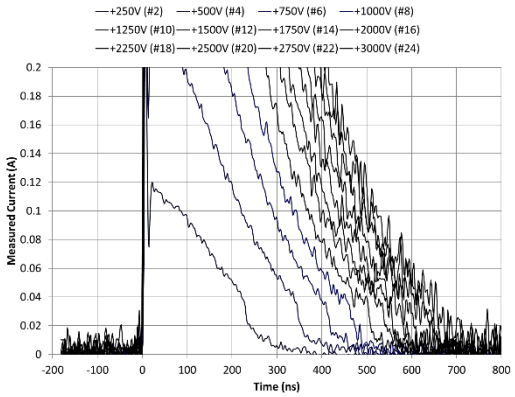

Fig. 12 HBM current versus time for SCR Design 1 with an expanded current scale

TLP results for SCR Design 2 are shown in Fig. 13. This SCR did not work as well as SCR Design 1. The breakdown voltage is about 48 V, followed by immediate damage to the device. The HBM data showed passing results at 250 V, minor damage at 500 V and 750 V, more damage at 1000 V and extensive damage at 1250 V. The use of a test structure to test this design saved a great deal of time and silicon area by not committing to a full protection strategy using this layout.

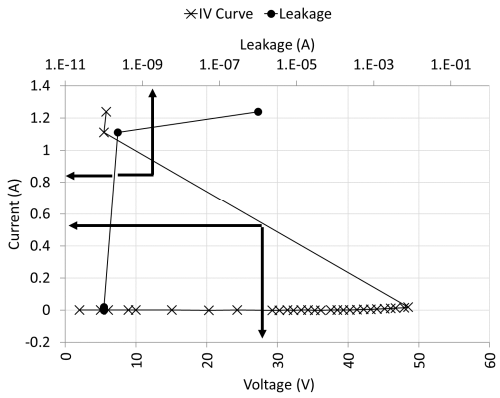

Fig. 13 TLP measurements of SCR Design 2

D. pnp

The final single element test structure is the pnp with the n base tied to one of the p diffusions. The TLP results are shown in Fig. 14. The TLP IV curve looks very similar to a reverse bias diode with a 31 V breakdown. The pnp structure, however, gives a lower dynamic resistance than would be seen for a similar sized diode. A linear fit to the pnp data was performed for the data between 10 mA and 100 mA, yielding a voltage intercept of 31.2 V and a dynamic resistance of 46.3 ohms. The 31.2 V breakdown is a good choice for protection of the nLDMOS device discussed earlier. 31.2 V is well above the expected 25 V working voltage for the transistor and well below the transistor's 48 V breakdown. The onset of damage at about 0.1 A for the pnp is not sufficient to provide adequate protection. The benefit of the pnp structure is that, since it has no snapback, multiple copies can be placed in parallel to improve the overall current carrying capability as well as reduced dynamic resistance. Using parallel devices, which have deep snapback such as SCRs, is often unsuccessful because once one finger of a multi finger device goes into snapback other fingers are prevented from going into snapback and the single finger must carry all of the current.

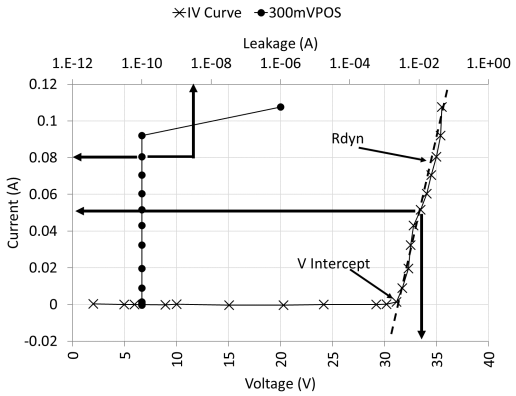

Fig. 14 TLP measurement of pnp device. The dashed line is a linear fit to the data over the range of 10 to 100 mA

E. Full Protection Design:

TLP data for a full protection design is shown in Fig. 15. The protection design consists of 26 parallel replications of the pnp device, discussed in section III.D, in series with 5 parallel replications of the p-NWELL diode, discussed in section III.A. 26 parallel pnp devices would be expected to carry up to 2.39 A of 100 ns long TLP current based on a single pnp being able to carry 92 mA. Similarly, 5 p-NWELL diodes in parallel should carry 10 A of 100 ns TLP current based on the 2 A capability of a single diode. The pnp is therefore the weaker element of the chain and should give a better prediction of the current carrying capability of the full protection device. The data in Fig. 15 shows the full protection device carrying 2.12 A of 100 ns TLP current without damage. This is slightly less than the predicted 2.39 A of current, but it is likely that individual elements in a closely packed array will not be able to carry as much current as an isolated device, due to lower ability to dissipate heat.

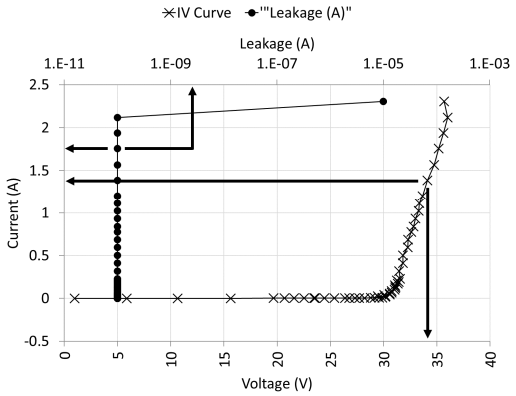

Fig. 15 TLP on full ESD protection structure using pnp devices

A linear fit of the data between 0.1 A and 2 A yields a voltage intercept of 30.8 and a dynamic resistance of 2.46 ohms. The HBM data showed passing results at 3800 V and failure at 4000 V. This is consistent with the earlier rule of thumb of 2 kV of HBM robustness for 1 A of survival for a 100 ns TLP pulse.

An advantage of the two-pin HBM system is that it is sometimes possible to pinpoint the exact time of failure during HBM testing by observing the measured voltage versus time curve. This is illustrated in Fig. 16 which shows the voltage captures for 3800 V, which did not cause damage, and for 4000 V, which resulted in damage. After an initial voltage spike, the voltage is clamped at about 35 V. For the 3800 V pulse the voltage remains clamped for the full duration of the measured waveform. At 4000 V the time of damage can be seen at 226 ns, when the voltage across the protection device drops from 35 V to about 3.5 V.

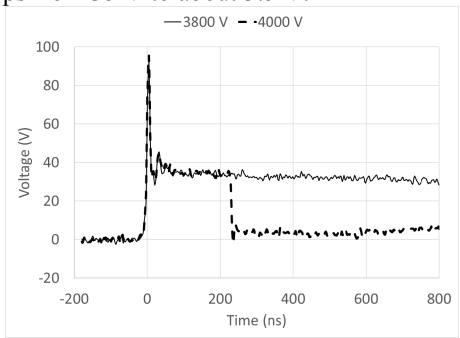

Fig. 16 Voltage capture on the 3800 V and 4000 V HBM pulses on the full protection design using the pnp structure

VI. CONCLUSIONS

This paper has presented TLP and HBM measurements on ESD test structures using a two-pin tester. The two-pin tester's unique ability to perform both measurements at wafer level, and its ability to measure voltage and current during HBM testing improves the usefulness of ESD test structures and can significantly shorten the design cycle.

TLP is usually performed at wafer level and provides high quality IV curves in which each data point is measured in the time domain of an ESD event. TLP IV curves yield important design parameters such as breakdown voltages and dynamic resistance. TLP data is also used to create model files, valid for the high currents and shorts times of ESD events.

As shown, TLP usually provides a good prediction of HBM pass/fail levels. 50-ohm TLP has limitation however, especially when measuring devices with snapback. Measuring voltage and current during each HBM pulse, supplements the TLP data and provides insight beyond the pass/fail data available from most HBM testers. HBM waveform measurements provide information on device performance during an exponential current decay, not available from TLP with its abrupt decay in current. HBM, with its 1500-ohm source impedance, can explore snapback behavior at lower currents than 50-ohm TLP. Additionally, two-pin testing provides data without the parasitic effects present in matrix based HBM test systems, and can be performed without expensive and time-consuming packaging and test board development.

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