Field Induced Charged Device Model: What really happens

Introduction

Integrated circuits are commonly tested for ESD robustness with 3 tests, Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM). Most engineers quickly grasp the procedure for HBM and MM but CDM is often poorly understood. This is unfortunate because a large fraction of the ESD failures experienced in modern board assembly operations are CDM type failures. This article will describe the events which occur during a CDM test conducted using the widely accepted field induced CDM (FCDM)[1,2] test and discuss some of the issues involved with the most widely used FCDM standards.

All ESD events consist of a charged object discharging through a discharge path. Characterizing an ESD event requires understanding both the capacitance and the discharge path. ESD stress tests such as HBM and MM can be described with the simple circuit diagram in Figure 1. This procedure works well because these test standards emulate a person or machine becoming charged and discharging through the sample being tested. The capacitance is a person for HBM (100pF) or the machine for MM (200pF). The discharge path for a human includes skin and body resistance which is approximated by a 1500Ω resistor. For a machine the current is limited by the induction in a metallic discharge path, about 0.8μH for the specified waveform. CDM is different. CDM emulates an integrated circuit that becomes charged during handling and discharges to a grounded metallic surface. The capacitance is the capacitance of the integrated circuit to its surroundings and the discharge path is a pin of the IC directly to a grounded surface. The test method for CDM must have a capacitance that scales with the device under test's (DUT) capacitance and a discharge path with very little impedance other than the DUT's own pin impedance.

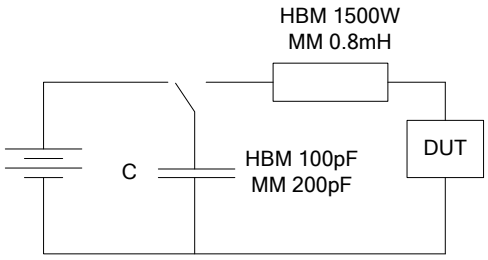

Figure 1 Basic circuit diagram used to describe HBM and MM

Figure 2 shows an FCDM simulator. The simulator consists of a metallic field plate that may or may not have a thin insulator on its surface. The presence, thickness and material of the insulator depend on the specific standard used. Differences between different FCDM standards will be discussed later. The potential of the field plate can be controlled with a high voltage power supply through a high value resistor. Suspended above the

field plate is a ground plane. At the center of the ground plane is a spring loaded pogo pin in the center of a 1Ω disk resistor connected to the ground plane. The pogo pin and ground plane are also connected to a 50Ω coaxial cable. The separation between the field plate and the ground plane as well as the relative position of the ground plane over the field plate is computer controlled.

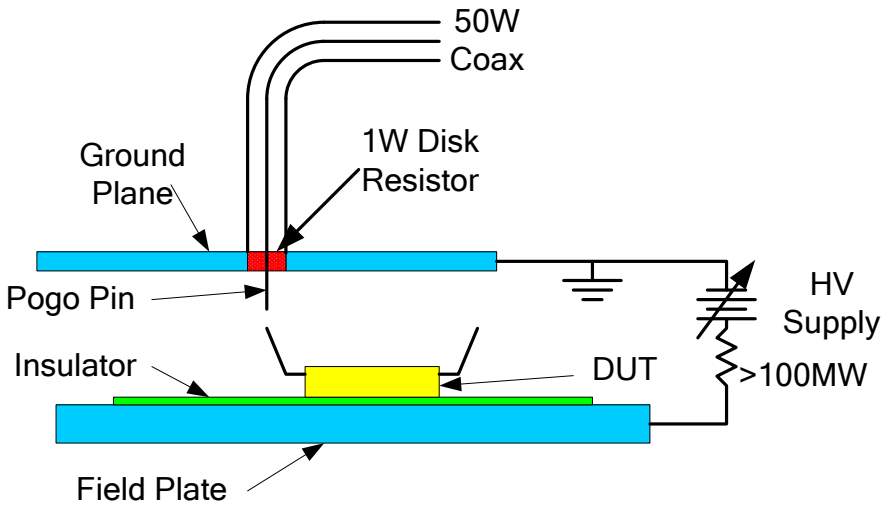

Figure 2 Field Induced Charged Device Model Simulator

Placing the DUT with the pin side up (dead bug position) produces a capacitance between the DUT and the field plate that scales with the size of the DUT. A low inductance discharge path to ground is formed by moving the ground plane relative to the field plate such that the pogo pin can touch any pin on the DUT. The 1Ω resistor and coaxial cable provide a low inductance current sensor so that discharge waveforms can be conveniently measured. The process of charging and discharging the DUT is where most of the confusion over FCDM occurs. Confusion about the test procedure is understandable because the actual process is opposite from what is expected. It is often stated that in FCDM the DUT is inductively charged and then discharged by contacting the pogo pin to the DUT. In fact field induction does not place any charge on the device. Also, the "discharge" when the pogo pin first touches the DUT is when the DUT is actually charged.

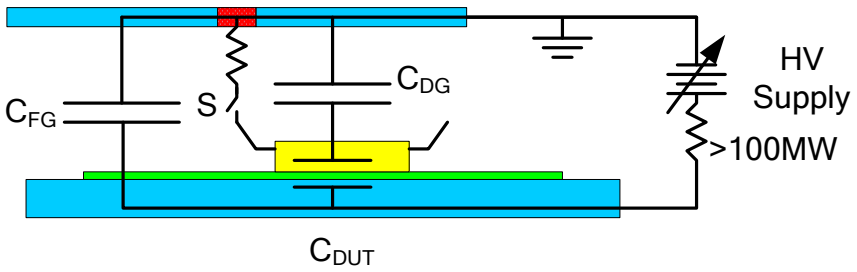

Figure 3 Capacitors added to field induced CDM simulator

In Figure 3 a circuit diagram is overlaid on top of a simplified version of the FCDM simulator. This circuit is a simplification of the full circuit but shows the most important features. A very thorough theoretical treatment of FCDM testing is provided by Atwood et. al.[3] C_{DUT} is the capacitance of the DUT to the field plate, C_{DG} is the capacitance of the DUT to the ground plane and C_{FG} is the capacitance of the field plate to the ground plane. Touching the pogo pin to a pin on the DUT has been represented by the switch S. Key to the understanding of FCDM is the series capacitors C_{DUT} and C_{DG}. Assuming no initial charge on the DUT, with the switch S open the DC voltage between the DUT and the Field Plate is:

$$V_{DUT} = \frac{C_{DG} * V_{HV}}{(C_{DG} + C_{DUT})}$$

Because the separation of the DUT from the field plate is always much less than the separation of the DUT from the ground plane; C_{DUT} is always much larger than C_{DG}. The potential of the DUT will therefore track the voltage on the power supply. The potential of the DUT relative to the ground plane can therefore be controlled without actually putting any net charge on the DUT.

There are two procedures for doing FCDM stressing. A positive and a negative stress can be performed with a single charging of the field plate or positive and negative stresses can be done separately. The two procedures start out the same. The single stress method will be described first, followed by the dual polarity stress.

1. With the field plate at zero volts an uncharged DUT is placed on the field plate in the dead bug position and the ground plane is positioned with the pogo pin above the pin to be tested.
2. The field plate is raised to a high potential, for example +500V. The high value resistor insures that the field plate changes potential relatively slowly. The slow change in potential insures that the DUT is not damaged before the CDM event. The potential of the DUT will closely track the field plate, reaching in excess of 450V, although there will be no net charge on the DUT.
3. After the voltage has stabilized the separation between the field plate and the ground plane is reduced until an arc forms between the pogo pin and the DUT pin

and eventually the two pins touch. This is equivalent to closing the switch S in Figure 3.

4. Closing S in the circuit diagram produces a very rapid grounding of the DUT and a redistribution of charge between the three capacitors. Only the 1Ω resistor, arc resistance and the inductance within the pogo pin and the DUT pin limit the current pulse. The peak current can be anywhere from a fraction of an Amp to 20A depending on the size of the DUT. At this point the DUT is charged and the potential between the field plate and the ground plane has fallen as the capacitor C_{FG} provides charge to the DUT. During this redistribution of charge, which lasts under 5ns, the high voltage power supply and the high value resistor can be ignored because of their slow response time.
5. After the initial redistribution of charge the field plate will slowly return to the voltage on the high voltage power supply, while the DUT remains at zero potential but in a charged state.

At this point the single pulse and dual pulse procedures begin to differ. We will continue with the single pulse procedure.

6. With the pogo pin still touching the DUT pin the HV power supply voltage is set to zero. The field plate will slowly return to zero volts and the charge on the DUT will slowly bleed off through the pogo pin.
7. When the field plate is at zero volts the distance between the field plate and ground plane can be returned to the original separation. At this point the procedure can be repeated for another stress on the same pin, a stress on the same pin with opposite polarity, or testing can be continued on a different DUT pin.

A sample FCDM waveform for a small JEDEC calibration module is shown in Figure 4. The waveform shows the typical CDM characteristic; a very high current short duration pulse.

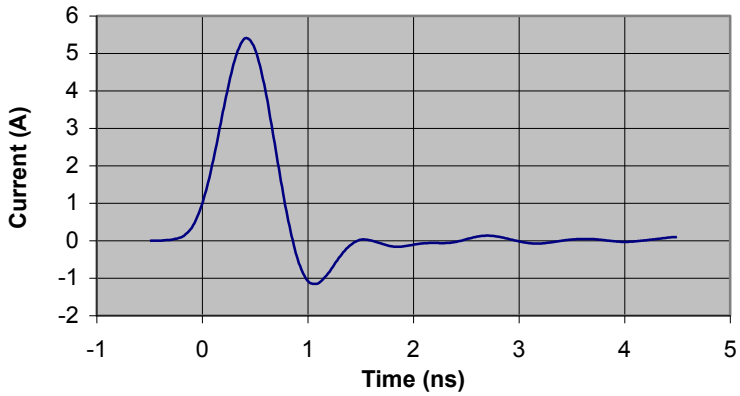

Figure 4 Field Induced CDM waveform of a small JEDEC Module at 500V

The dual pulse procedure continues after step 5 of the single polarity procedure.

6. Without changing the voltage on the HV power supply the distance between the field plate and the ground plane is increased so that the pogo pin separates from the DUT pin. The DUT is still charged and will stay at approximately zero volts while the field plate is at the HV power supply voltage.
7. The potential on the field plate is slowly returned to zero by setting the HV supply to 0V. Changing the field plate potential to zero volts does not change the fact that there is a nearly 500V potential across the capacitor C_{DUT}. The result is that when the field plate reaches zero volts, the DUT potential is close to -500V.
8. At this point the separation of the field plate and ground plane is decreased until an arc forms between the pogo pin and the DUT pin, rapidly grounding the DUT. This results in a second stress pulse with approximately equal amplitude as the first, but opposite polarity.
9. After a suitable delay, to allow the field plate to return to zero volts after the arc, the separation between the field plate and the ground plane is increased and the test sequence is complete. Further stresses can be performed on the same pin or testing can be continued on other DUT pins.

The dual pulse method can save some time during FCDM testing.

FCDM Standards

Three standards bodies issue CDM measurement standards using the FCDM method, JEDEC,[1] the Electrostatic Discharge Association (ESDA),[2] and Automotive Electronics Council (AEC).[4] The AEC standard closely follows the ESDA standard and will not be discussed explicitly. While the JEDEC and ESDA standards are similar in many ways there are several features that differ, as illustrated in

Table 1. The result is that failure levels measured with the different standards can not be considered equivalent. This is in contrast to HBM and MM where the standards issued by the different organizations are similar enough that test results can be considered directly comparable. One of the main differences is that JEDEC requires a 0.381mm thick insulator on the field plate while ESDA requires either no insulator or a very thin insulator. The capacitance C_{DUT} will therefore be larger for a system built for the ESDA standard. Each standard specifies a pair of calibration modules to be used for waveform verification. The modules and the required waveform parameters are different for the two standards. The JEDEC modules are coin shaped disks while ESDA uses a metal film on top of a 0.8mm thick sheet of an FR-4 circuit board.

Table 1 Comparison of JEDEC and ESDA FCDM standards

Organization	JEDEC	ESDA
Standard	JESD22-C101C	JESD22-C101C
Insulator Thickness (mm)	0.381 ± 0.038	No Insulator or ≤ 0.13
Insulator Dielectric Constant	4.7 ±5%	Not Specified
Calibration Modules	Metal Coins	Metal Film on 0.8mm Thick FR-4
Nominal Module Capacitance pF	6.8 & 55	4 & 30
Peak Current (1GHz oscilloscope) (A)	5.75 & 11.5 (±15%)	4.5 &14 (±20%)

Summary

FCDM is an extremely valuable test method for insuring that integrated circuits can survive in a modern, automated manufacturing environment. The test method creates a capacitance that scales with DUT size and a low impedance discharge path, providing a good simulation of real CDM events. The two leading FDCM standards, JEDEC and ESDA, are very similar but have differences in their details that make their test results somewhat different. While the ESDA stress is often considered more severe, there is no simple correlation factor between the test results.

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[1] JEDEC, "Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components", JESD22-C101C Dec. 2004, JSSTA.
[2] ESDA, "ESD Association Standard Test Method STM5.3.1-1999", ESD Association, 1999.
[3] B.C. Atwood, Y. Zhou , D. Clarke, T Weyl, "Effect of Large Device Capacitance on FICDM Peak Current" EOS/ESD Symposium, 2007.
[4] AEC "Charged Device Model (CDM) Electrostatic Discharge (ESD) Test" AEC - Q100-011 Rev-B July 18, 2003.