Cover Story

The Future of ESD Testing

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Predicting the future is a hazardous but useful exercise. Predicting the future involves evaluating the issues of today and anticipating how those issues will influence the decisions made by a variety of people. These decisions map the future.

The future of ESD testing will be determined by standards bodies trying to write technically sound test methods, manufacturers that want reliable tests but have considerable economic constraints, and purchasers of electronic systems and components desiring high quality and reliability products at the lowest possible cost.

This article will try to peer into the future by assessing what is happening today in the field of ESD testing.

ESD testing is divided into two categories. Traditionally, device-level testing evaluates components such as integrated circuits to determine their ability to survive the manufacturing process in ESD-controlled areas. System-level testing is done to determine if systems can survive ESD events in the real world, where there is no attempt to limit exposure to ESD events.

There is, however, a grey area developing between device-level and system-level testing. Original equipment makers (OEM) want to predict system-level ESD robustness based on device-level capability. OEMs are therefore asking suppliers to do system-level ESD stress on components.

This article will deal with the two areas of ESD testing, but will also reflect on how the grey area between device and system test is affecting our future. We will first discuss device-level testing, focusing first on a movement to define more realistic target levels for device testing, and then discuss individual device tests. System-level testing, and how it will influence device-level testing, will then be discussed. This is intended to be a practical view of the future and will not try to speculate on the perfect ESD test which is "just around the corner," since it is doubtful that we will ever develop such a test.

Device-Level Testing

A recent development that will influence the future of device-level ESD testing is a working relationship between the Electrostatic Discharge Association (ESDA) and JEDEC to jointly develop device testing standards. This agreement will eventually produce joint standards for human body model (HBM) testing and charged device model (CDM) testing, greatly simplifying the testing environment and also precluding the development of competing test methods for cable discharge event (CDE) and human metal model (HMM), which could have developed without this agreement.

Required ESD Levels for Devices

Integrated circuits (IC) are tested for ESD robustness using one or more of the three device-level ESD tests, HBM, CDM, and machine model (MM). These tests are intended to ensure that the circuits can survive the manufacturing process. Which tests are performed and the passing level required is usually set between the manufacturer and purchaser of the circuit. The most commonly required passing voltages are 2000V for HBM, 500V for CDM and 200V for MM.

As integrated circuit technologies have advanced and performance demands have increased, it has become increasingly difficult to meet these passing levels. In many instances, exceptions to these passing levels have been allowed. Experience has shown that the lower passing level product did not have higher failure levels if basic ESD control procedures were employed during their manufacture. IC customers, however, have continued to request the commonly accepted ESD voltage levels, under the impression that higher levels must be better. The effort to meet the commonly accepted ESD passing levels costs considerable money due to redesign and product delays.

The Industry Council on ESD Target Levels was formed to determine what level of ESD robustness is required to survive the manufacturing process, and to recommend safe but realistic ESD target levels. It is a group of experts representing major IC manufacturers, contract manufacturers (CMs), ESD tester manufacturers, ESD consultants and ESD IP companies. Setting realistic goals will save money by not requiring unnecessary redesigns, thereby improving time to market without compromising yields in the manufacturing process.

The Council's first project was the release of a white paper on HBM and MM testing.[1] This document showed considerable data on the failure rates during manufacture for ICs with different levels of HBM and MM passing voltages. Based on this data, the Council recommended an HBM passing level of 1000V HBM.

The Council also recommended a de-emphasis on MM testing. The Council's data indicated that ICs that pass 1000 V HBM will have at least 30 V MM robustness, but could have MM robustness much higher than that. The data also showed 30 V of MM robustness was sufficient for high yield in a quality manufacturing environment.

The Industry Council is currently educating the electronics industry about their recommendations for HBM and MM, and the advantages for both IC suppliers and OEMs if more reasonable ESD target levels were adopted. The Council is beginning to have success, and it is anticipated that 1000V HBM will soon become the generally accepted value for HBM testing. As the industry becomes comfortable with this level, and as integrated circuit technologies continue to advance and performance goals increase, it is likely that even 500 V will become a commonly accepted value for HBM acceptance.

The second activity of the Industry Council is the development of a white paper on recommended CDM target levels. This is likely to be a bigger challenge than the white

paper on HBM and MM, since CDM testing is more challenging. There are several CDM test methods that produce different failure levels. Additionally, the size of the IC changes the stress experienced during a CDM event. It is anticipated the Council will need to make a recommendation that goes beyond adjusting the commonly accepted passing level to a new voltage.

Human Body Model (HBM)

HBM is the most mature of the device-level ESD test methods. As we discussed in a previous article (see *Conformity*, June 2008), there are still areas that present challenges for HBM testing. [2] The joint standards development effort between JEDEC and ESDA is currently addressing the HBM standard. At present, an ad hoc committee from both groups is addressing the technical issues where the two standards differ, and will shortly start to draft the joint standard.

That joint document will not be a major issue for the industry. There will likely be small changes in calibration procedure and other procedural changes, but there will not be a change in the pass/fail levels when the new document is adopted. The two test methods never differed in significant ways and a harmonization effort was undertaken several years ago. Some of the more challenging aspects of HBM testing will not be addressed by the joint committee until a merged document is available.

Modern high pin count products with a large number of independent power and ground pin groups employed to reduce noise present a challenge in testing. Test times increase dramatically, and current paths are stressed hundreds or thousands of times, leading to wear-out. HBM is intended to ensure that an integrated circuit can survive at most a handful of ESD stresses during manufacture. The challenge is to ensure that there are no weak pin combinations, without excessive test times and wear-out.

There are several methods that can be used to address excessive test times and wear-out. There is a provision in the JEDEC test method, but not in the ESDA method, that can be used to at least partially address both the wear-out and test time issues. If an IC uses power planes within a package to short all of the pins within a power or ground group together, a single pin may be chosen to represent the stress on the entire group. This will be an area of potential interest when the joint ESDA/JEDEC standard is issued.

Another method that could be used to deal with the long test times and wear-out issues is to modify the pin combinations in HBM. Modifications of HBM pin combinations have been discussed in the available literature [3], and it is expected that there will be considerable deliberation on this approach in future standards development efforts.

There are two basic types of pin combinations done during HBM testing. In one stress type, each input/output pin is stressed while all other inputs and outputs are grounded. In the second type of stress (and the most time consuming to conduct), each power supply and ground group is grounded while all other pins on the circuit are stressed, one at a time.

This second stress type is illustrated in Figure 1 using a typical steering diode and power supply protection strategy. Consider the stressing of the input pin I1 positive versus the ground pin group VSS2. The intended current path is red in Figure 1; from pin I1, through the forward biased diode to VDD1, through the VDD1 to VSS1 power supply protection and finally through the forward biased diode between VSS1 and VSS2.

Elements of this current path are stressed multiple times during the full testing of the integrated circuit. For example, I1 to VDD1, green, I1 to VSS1, blue, VDD1 to VSS1, pink, and VSS1 to VSS2, black. It can be argued that this is overkill. One suggestion that has been made is to stress only inputs to their local power supply. In the example in Figure 1, I1 would only be stressed to VDD1 and VSS1. Stressing between I1 to VSS2 and VDD2 would be eliminated because stressing from VDD1 and VSS1 to VSS2 and VDD2 would cover the remainder of the current paths.

This approach would significantly reduce test times as well as reduce wear-out. Data needs to be provided before such a sequence will be supported by many customers, but we predict that this type of reduced pin combination will become more commonplace in the future.

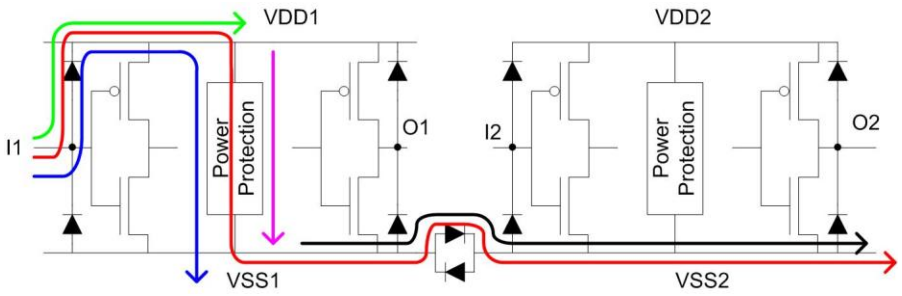

Figure 1: HBM stress from I1 to VSS2.

Tester parasitics interacting with the device under test have been shown to result in unexpected failures, as discussed in [2]. The failures occur because the interaction between the tester and the device creates a stress quite different from the intended HBM stress. To date, it has required extensive engineering effort and judgment to resolve the problem. After extensive work, the debate has often been, did the IC pass the test?

The obvious answer to this dilemma is to build new HBM testers that remove the parasitics. This is both obvious and, we believe, unlikely, since the current generation of relay matrix-based HBM test systems are, in general, serving the industry well. In most situations, the test results are as expected, or can be explained without invoking tester issues. The relay matrix systems are fast, which is a necessary feature with the high pin count devices that are increasingly being produced. There are currently no low parasitic tester ideas that have the speed needed to address the issues of modern high pin count ICs.

We anticipate that failures due to tester parasitic issues will continue to be addressed on a case-by-case base for the foreseeable future. We anticipate that standards bodies will provide some guidance on acceptable alternative pin combinations to reduce the problems due to tester parasitics.

Charged Device Mode (CDM)

CDM is a test method that may see considerable change over the next few years. The details of field-induced CDM (FCDM) are covered in [4]. The joint standards effort between JEDEC and ESDA will be part of this change. The two test methods are conceptually identical but differ in significant details. The insulator thickness between the device under test and the field plate is different, the test modules to calibrate the systems are different, and there are differences in the required waveforms.

The result is that ICs tested according to both standards do not receive the same passing voltage levels. The ESDA test method is usually considered the more severe stress, resulting in lower passing voltages. Merging the test methods will be a challenge when there is often no clear cut technical advantage of one method over the other.

Complicating this is that the merged test method will likely produce a change in the passing voltage when users move to the new standard. Maintaining dual standards is not, however, a good long term practice for the industry.

As discussed above, the Industry Council on ESD Target Levels is now focusing on CDM. Their recommendation, and the industry's reaction to the recommendation, will greatly influence the future of CDM testing. Their recommendation may significantly change how CDM data is viewed and interpreted. A change in how product is qualified is usually met with considerable reluctance and this may be no exception. The good news is that any recommendation by the Council will be backed by considerable real world manufacturing data, as was their recommendation for HBM.

There are also some basic concerns about the field-induced CDM method used in both the JEDEC and ESDA test methods. FCDM uses an air discharge to initiate the stress. Air discharge can vary considerably, and atmospheric conditions such as temperature, humidity and pressure all affect the test results. The shape and cleanliness of the probe tip that initiates the air discharge between the test head and the device under test also has a significant effect on the size of the stress current pulse.

These factors combine to produce a wide scatter in the stress current, resulting in more variability in the test results than is considered acceptable by many test engineers. There is considerable interest in an arc free CDM test which maintains the speed of the current FCDM test method.

An alternative method for producing a CDM speed current pulse without an air discharge, as well as without a relay that will slow the pulse shape, is capacitively coupled transmission line pulse (CC-TLP). The basic concept is shown in Figure 2.

An IC is placed pin side up on top of a thin insulator on a grounded metal field plate. A coaxial probe touches the pin to be tested. A voltage pulse, produced by a very fast transmission line pulse system, will inject a current pulse dependent not only on the properties of the voltage pulse but also proportional to the capacitance between the IC and the field plate.

A number of papers have been published on this subject. A CDM tester based on this technique would remove the problems inherent in an air discharge test method, and should be relatively straightforward to automate. Test time with an automated system of this type should be similar to those for current FCDM testers. We predict that there will be increased interest in some form of cc-TLP to replace FCDM testing.

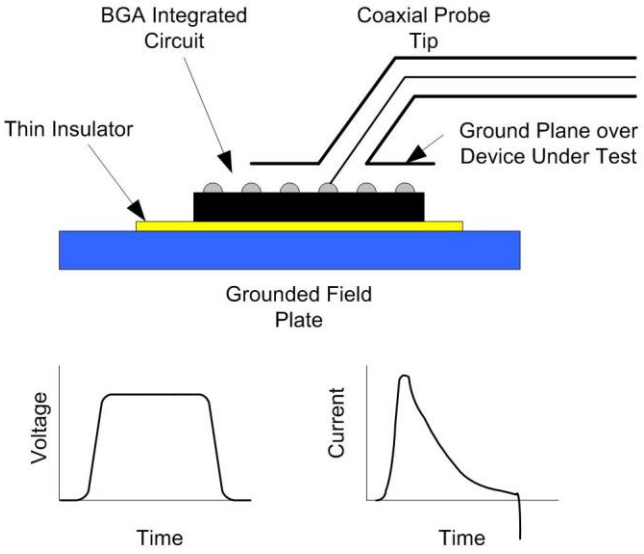

Figure 1: Capacitively coupled TLP, simplified test setup, stress voltage for 50 Ω load, and current into integrated circuit during cc-TLP (a technical correction has been made from the original published figure)

Machine Model (MM)

Machine model testing will likely continue to experience a slow decline in use. There is no active effort within either ESDA or JEDEC to update the test method documents. JESD47E [6], the JEDEC document specifying stress tests that should be done to integrated circuits for qualification, has not recommended MM testing for a number of years.

Even in the automobile industry, where MM has always been popular, it is not required. AEC-Q100-Rev-F requires that either HBM or MM be done, whereas CDM must be done. The Industry Council, in its white paper on recommended passing levels for HBM and MM, downplayed testing with machine model. Many companies, however, have extensive history of MM results for which they have developed confidence. It is unlikely that MM testing will be discontinued suddenly.

System-Level Testing

Most system-level testing is done using the IEC 61000-4-2 test method, in which systems are tested using a hand-held ESD gun. Discussion of system-level ESD testing waveforms and the test setup can be found in [8] and [9]. A new update to this standard is promised, but it is not likely that the new update will result in major changes in how systems are supposed to be tested. The changes are likely to concentrate on improving the measurement and definition of the stress waveform.

We believe that some of the biggest changes in ESD testing will be in those areas where IEC 61000-4-2 is being applied outside of its intended scope. IEC 61000-4-2 specifically states that one is not to do contact discharge with the ESD gun onto the pins of system connectors, such as Ethernet ports or USB ports. If the connector has a metal shell, contact discharge should be done directly to the metal shell. If the connector has an insulating shell, air discharge should be done to the region of the connector.

Despite this, there are regular reports of contact discharge being performed directly to the pins of a system. The motivation is often to measure some form of robustness due to the cable discharge event (CDE). CDE occurs when a cable becomes charged due to friction and then discharges as it is plugged into a system. This is a common event, but there is no generally accepted test method. A number of companies have internal test methods, but none has been made available to the industry. The result is an undisciplined approach to defining robustness for this real world stress.

The ESDA Working Group 14 is currently working on a test procedure for CDE that should be available for industry review within the next year. It is hoped that this test procedure will provide a common test procedure for the industry.

A second area where IEC 61000-4-2 is used outside of its scope is the testing of components. OEMs need their products to pass system-level ESD testing, and they are increasingly looking toward their suppliers to help them in this effort. OEMs are increasingly asking their suppliers to provide components that pass a high level of IEC 61000-4-2 stress, often 8 kV contact discharge and 15 kV air discharge. This is being requested despite the fact that IEC 61000-4-2 does not cover the testing of components. IEC 61000-4-2 does not specify the following important test parameters for component testing:

- How to apply stress;
- Required test fixtures;
- Grounding for the ESD gun and component under test;
- Pins requiring stress;
- Should the component be powered during the test;
- Should the component be functioning during the test;
- The definition of failure;
- How to verify the component was stressed.

Component suppliers have struggled to determine how to meet their customer's requirements without the guidance of a standard, resulting in inconsistency between suppliers. Only recently have standards bodies responded. For example, IEC has issued a test method limited to CAN bus transceivers, used in the automotive industry, IEC 62228. [10]

In addition, ESDA working group 5.6 is now working on a more general test procedure which should be available for industry review within the next year. This new test method has been named human metal model, (HMM). This is because the original IEC 61000-4-2 current waveform is intended to simulate a charged person, holding a metal object such as a screwdriver or key, discharging to a grounded object. Discharge from the metal object produces the initial current spike, while the remainder of the waveform is the discharge of the person.

Summary

In the next few years, the electronics industry will become increasingly aware that advanced integrated circuits can be reliably handled at lower ESD passing voltages for HBM, and with revised targets for CDM. The increased care in handling of these advanced products will be more than made up for by lower costs due to fewer redesigns, improved time to market, and higher performance products. The MM will slowly fade from use, but will not disappear for several years, if ever. A generally accepted CDE test will be available for system testing. This test will replace the proprietary tests used by several companies. Claims that components can pass the IEC 61000-4-2 system-level test will be replaced with better defined specifications based on IEC 62228 for the CAN bus, or a more general HMM specification from the ESDA working group 5.6.

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References

1. Industry Council on ESD Target Levels, "White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements" August 2007, http://www.esdtargets.blogspot.com/.
2. Robert Ashton, "Human Body Model, The Hidden Challenges", Conformity, June 2008, pg. 32.
3. R. Gaertner, R. Aburano(1), T. Brodbeck, H. Gossner, J. Schaafhausen, W. Stadler, F. Zaengl, "Partitioned HBM Test - A New Method To Perform HBM Tests On Complex Devices", EOS/ESD Symposium 2005, pg 178.
4. Robert Ashton, "Field- Induced Charged Device Model: What Really Happens", Conformity, March 2008, pg 34.
5. H. Wolf, H. Gieser, W. Stadler, and W. Wilkening, "Capacitively coupled Transmission Line Pulsing, CC-TLP – A Traceable and Reproducible Stress Method in the CDM-Domain", EOS/ESD Symposium Proceedings, September, 2003.

6. JESD47E “Stress Driven Qualification of Integrated Circuits” January 2007.
7. AEC-Q100-Rev-F “Stress Test Qualification of Integrated Circuits”, Automotive Electronics Council 2003.
8. Robert Ashton, “System Level ESD Testing: The Waveforms”, Conformity, October 2007, pg. 28.
9. Robert Ashton, System level ESD Testing: The Test Setup”, Conformity, December 2007, pg. 34.
10. IEC TS 62228, “Integrated circuits – EMC evaluation of CAN transceivers”, International Electrotechnical Commission, February 2007.