Challenges in Testing

Human Body Model (HBM): The Hidden Challenges

Robert Ashton, ON Semiconductor

Human Body Model (HBM) is the oldest of the ESD test methods for testing integrated circuits. It is hard to overestimate the positive impact that this test method has had on the electronics industry. Without the ESD robustness built into electronic components in order to pass this test, there certainly would be enormous expenditures to deal with components damaged by ESD during manufacture.

However, the HBM standard was developed in the 1970s and 1980s when integrated circuits had far fewer pins and only one or two power supplies. As integrated circuits have grown in complexity and performance, the basic HBM standard has been applied to the newer circuits. This has only been possible with the introduction of increasingly more sophisticated and complex automated HBM simulators, able to handle in excess of 2000 pins. (In ESD terminology an HBM simulator is a machine that delivers a stress pulse to simulate an ESD event. It is not a computer program.)

The combination of sophisticated test equipment and modern integrated circuits with lower operating voltages and multiple power supplies, each with many parallel pins, has resulted in some "unintended consequences." This article will review the basics of the HBM test method, and some of the issues that have arisen over the years as HBM has been performed on newer and newer technologies. Issues that will be discussed include, long test times, wear out, "trailing pulse," "pre-pulse voltage," parasitic effects due to test sample to test system interaction, and acceptable qualification levels.

HBM Basics

The basic circuit model is shown in Figure 1. A 100pF capacitor is discharged through a 1500 Ω resistor and the device under test (DUT). The test system is calibrated by measuring the current through a short and a 500 Ω resistor. The required waveform for a short includes a 2 to 10 ns rise time, a peak current that scales with voltage, a nominal 150 ns decay time and ringing not to exceed 15% of the peak current. The waveform requirements are detailed in the test standards by JEDEC [1] and ESDA [2]. A sample HBM waveform into a short for 2000V is shown in Figure 2.

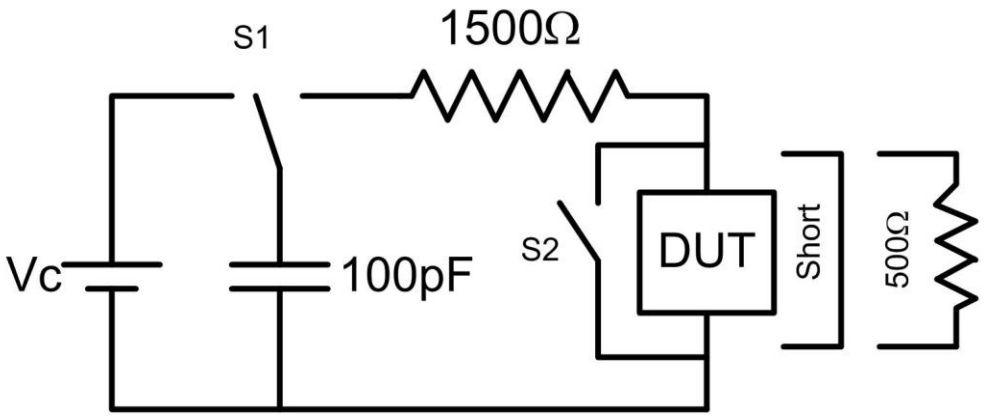

Figure 1: Basic HBM Schematic. S1 initiates the stress pulse and S2 is used to remove built up charge after the stress through a high resistance.

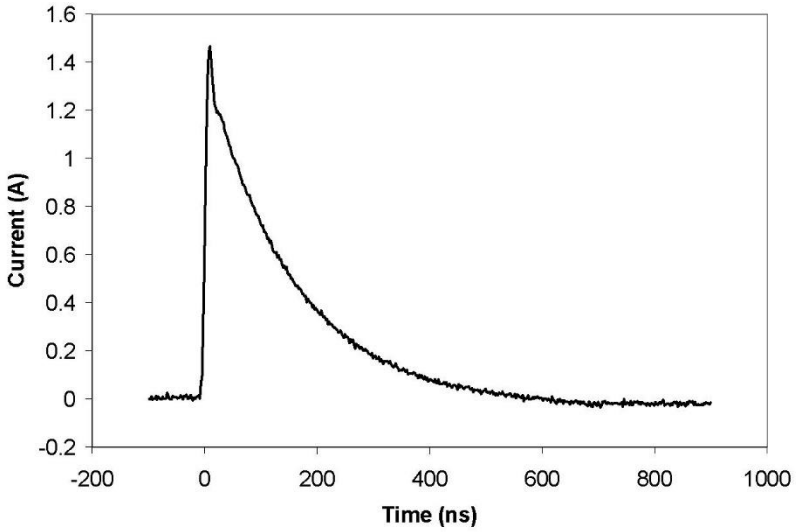

Figure 2: Measured HBM waveform for 2000V into a short

The pin combinations for HBM testing are described in Table 1. A power supply group is any group of pins metallically connected in the integrated circuit package or on the die and providing power to the circuit. Ground pins are considered power supply pins. The intent of the pin combinations in Table 1 is to stress all current paths that could experience ESD stress.

Pin Combination	Grounded Pins	Stress Pins	Floating Pins
1	Supply Group 1	All pins not grounded, one at a time	All pins not in Supply Group 1 and not under test
2	Supply Group 2	All pins not grounded, one at a time	All pins not in Supply Group 2 and not under test
i	Supply Group i	All pins not grounded, one at a time	All pins not in Supply Group i and not under test
n	Supply Group n	All pins not grounded, one at a time	All pins not in Supply Group n and not under test
n+1	All I/O except stressed I/O	Each I/O pin, one at a time	All Supply Pins

Table 1: Pin Combinations for HBM testing for an integrated circuit with n power supply groups

Test Time

The test time for HBM has risen dramatically in recent years. Part of the problem is increased number of pins, but more significant is the increase in the number of power pin groups. Consider a 500 pin device with 2 40 pin power groups for power and ground. A full stressing of this circuit requires 2680 stresses (1340 positive and 1340 negative). If the design is changed to separate out a single power and a single ground pin to provide quiet power to a small but critical circuit, the number of stresses increases to 4680 (2340 positive and 2340 negative).

Today many integrated circuits have 40 or 50 or more separate power supply groups. The result is 10s or 100s of thousands of individual stresses and many hours of test time. Long test time has been addressed in the standards by reducing the number of stresses from 3 to 1, and by reducing the delay between stresses from 1 second to 0.3 seconds and even 0.1 seconds in the latest JEDEC standard. Long test time remains an issue.

Wear Out

The intent of HBM testing is to ensure that an integrated circuit can survive the manufacturing process. Once the integrated circuit is within a completed system, the system should provide ESD protection. All electronic manufacturing is done in ESD controlled areas to reduce the number and severity of ESD events. Without ESD controls, even products that can survive 2000V of HBM stress would not survive manufacture.

An integrated circuit, in its entire lifetime, is not expected to experience more than a handful of ESD events of modest severity. HBM testing, in its attempt at thoroughness, exposes the circuit to many more stresses than a circuit will experience in a typical

lifetime. Each of the HBM stresses does exercise a unique current path, but parts of paths will be stressed repeatedly. It is well known in the ESD community that wear-out is an issue, but there is almost nothing in the literature documenting it formally.

Stress Count Reduction

Excessive test time and wear-out are technically different issues, but the solutions are often related. Wear out is often dealt with by dividing testing between a number of samples. Rather than doing all pin combinations on each sample, subsets of the pin combinations are done on separate samples. This procedure increases the amount of handling during testing, but can significantly reduce the number of stresses individual samples experience. Test time is obviously not improved and more samples are needed for testing. Dividing the pin combinations across a number of samples can also be very useful in the case of failure, since the pin combinations that could have caused a failure are greatly reduced.

A recent change in the JEDEC HBM standard has had a beneficial impact on both test time and wear-out. Most very high pin count integrated circuits are packaged in ball grid array (BGA) packages. BGA packages are typically made on a circuit board-like substrate, with many separate interconnect layers. Power pin groups with multiple balls are usually shorted together with a power plane on one of the BGA's layers. When this is done the resistance between different pins in the same power pin group is very low. Stressing any single pin within the power pin group should be equivalent to stressing any of the other pins.

Under these conditions the JEDEC HBM standard allows a single pin of a power pin group to represent the entire power pin group. This change can significantly reduce test time in some designs and also greatly reduce repetitive stressing to the device. Integrated circuits that do not have a package power plane cannot use this technique because on the die metal connections can amount to several Ohms of resistance, making different pins within the power pin group not identical.

A method that has been proposed that would reduce both test time and wear-out is the partitioned HBM test.[3] This method significantly modifies the pin combinations as presented in Table 1. Testing is divided up into three partitions, with separate samples for each of the partitions. The intra-domain partition stresses all pins within power domains, but does no stressing between power domains. The inter-domain partition stresses all power and ground pins with respect to each other. The final partition stresses each signal pin against all other signal pins.

In the partition method, signal pins are never stressed with respect to power pin groups that do not supply the signal pin buffers. Users of this method report that circuits with high numbers of power domains have similar failure levels as circuits with fewer power domains, indicating less wear-out. It is also reported that the method is very effective at indicating the location of ESD weak circuits. The method cannot, however, be considered in full compliance with the HBM standards at this time.

Trailing Pulse

Several years ago, Texas Instruments traced a subtle degradation from ESD stress to small currents that flowed into the device under test from the HBM simulator many microseconds after the HBM current pulse.[4] The currents only affected advanced technologies with thin gate oxides, and were only present in some HBM simulator models. The currents were traced to ionized gas in the relay S1 in Figure 1. The ionized gas provided a current path between the high voltage power supply and the device under test.

Since then, the HBM standards have added a test to detect the presence of this current, and pulse source upgrades have become available for some HBM simulators that exhibited the problem. [1] The standards have not required that all HBM simulators remove the current because many IC technologies are not affected by the current. For advanced CMOS technologies, it is important to determine if the HBM simulator being used is free from the trailing current.

Pre Pulse Voltage

In the same period that the trailing pulse was discovered, another HBM simulator effect was discovered, the pre pulse voltage. [5] During an investigation of unexpected failures of ESD power supply protection circuits, it was discovered that several volts could build up across a device under test if the pin combination had high impedance and low capacitance. Under these conditions, some dynamic power supply clamps did not turn on. (The pre pulse voltage will be the subject of a future article in *Conformity* and will not be discussed further here.)

HBM Simulator Parasitics

HBM stressing of integrated circuits with hundreds of pins can not be done without automated test equipment. A conceptual schematic of a relay matrix HBM simulator is shown in Figure 3. Automated HBM simulators allow a stress pulse to be applied to any pin on the circuit and for one or more pins to be connected to the ground terminal, while the remaining pins remain floating. Not shown in Figure 3 are the circuits and relays needed to accommodate the leakage measurements circuitry present in most automated HBM simulators.

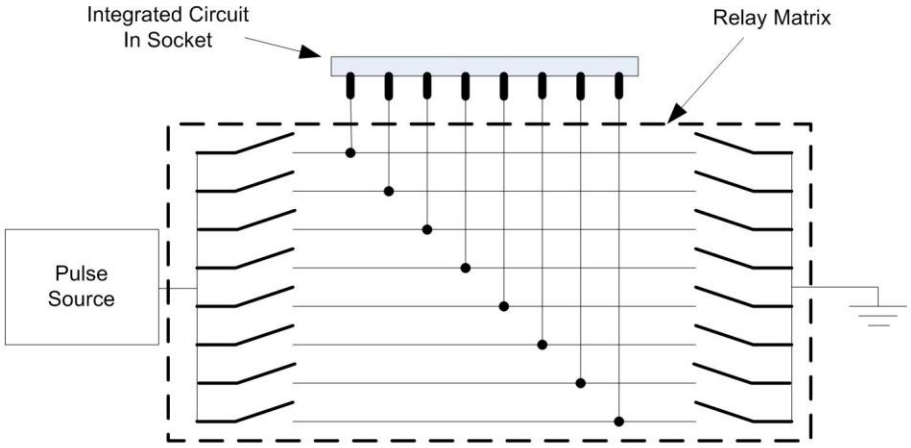

Figure 3: Conceptual schematic of relay matrix based automated HBM simulator

Automated HBM simulators have been extremely successful at allowing HBM stressing to be done on high pin count circuits in an efficient and reliable manner. Occasional reports, however, indicated that in some cases interactions between the automated simulators and the circuit under test resulted in unexpected results. [6] This led to the ESDA HBM working group, WG5.1, to investigate the behavior of a number of commonly used automated HBM simulators.[7] The method used was to employ special shorting modules that would short a number of simulator channels together and also had a wire loop that could accommodate a high speed current probe. The method is illustrated in Figure 4.

Figure 4 shows two wire loops and current probes to show how the short module could be used to measure current coming into the short module (the A side) or leaving the short module (the B side). Short modules from 14 pins to 256 pins were used in a combination of DIP and PGA form factors. It was found that, as the number of shorting pins increased, there was very little difference in the A side current, while there was significant reduction in the peak B side current and a large increase in the rise time as seen in Figure 5.

Figure 6 illustrates how the A and B currents can differ. Each of the "unused" channels of the HBM simulator includes parasitic capacitances across the open relays. The connection between the relays and the ground terminal is also not zero Ohms and the deviation is likely much larger than wiring resistance. HBM simulator manufacturers build machines that provide the waveforms specified in the HBM standards. They are not required to reproduce the HBM schematic as shown in Figure 1. This gives the manufacturer the design space to meet the waveform requirements.

One of the challenges is to prevent excess ringing during the stress. To do this it is likely that termination resistors have been added between the relays and the system ground. Reference [7] determined that the relay capacitance on modern high pin count HMB simulators ranged from 4.5 to 9 pF, and the termination resistance was likely in the range

of 50 to 100 Ohms. As an example, we will assume 7.5pF of relay capacitance and 75 Ω of termination resistance.

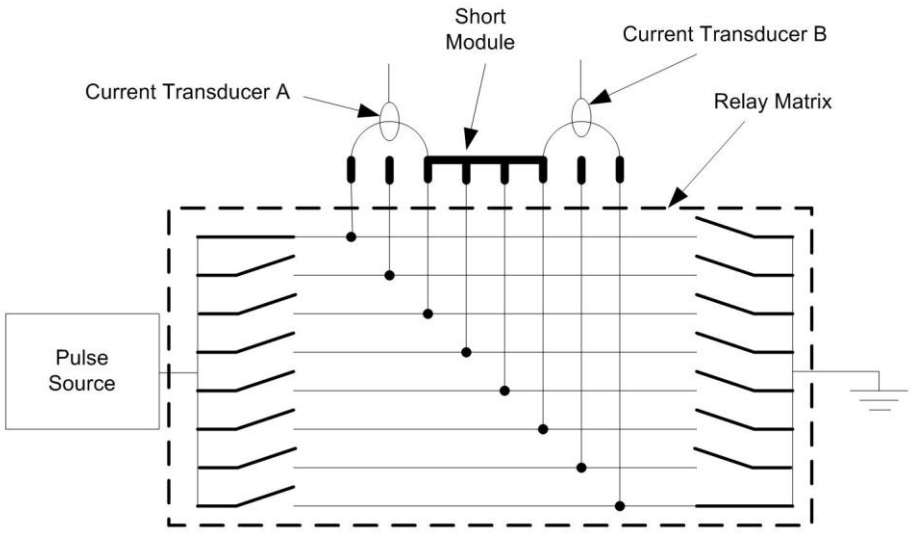

Figure 4: Measurement of input and output waveforms with a short module

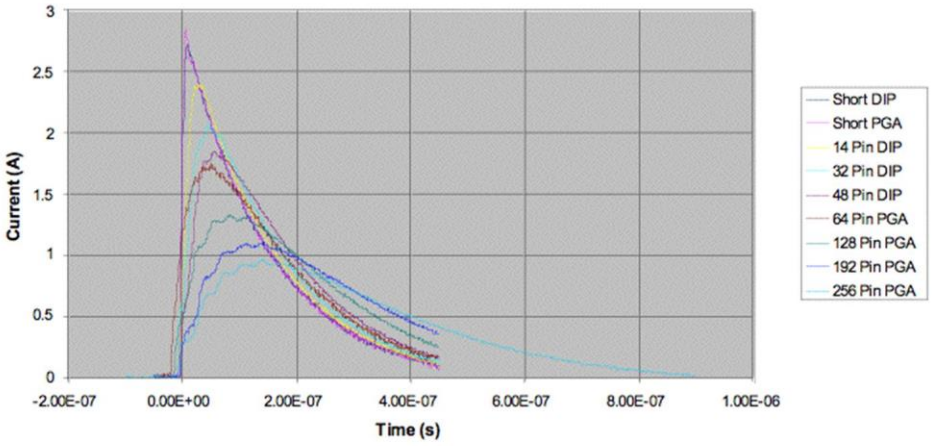

Figure 5: Measurement of B side current as a function of the number of pins

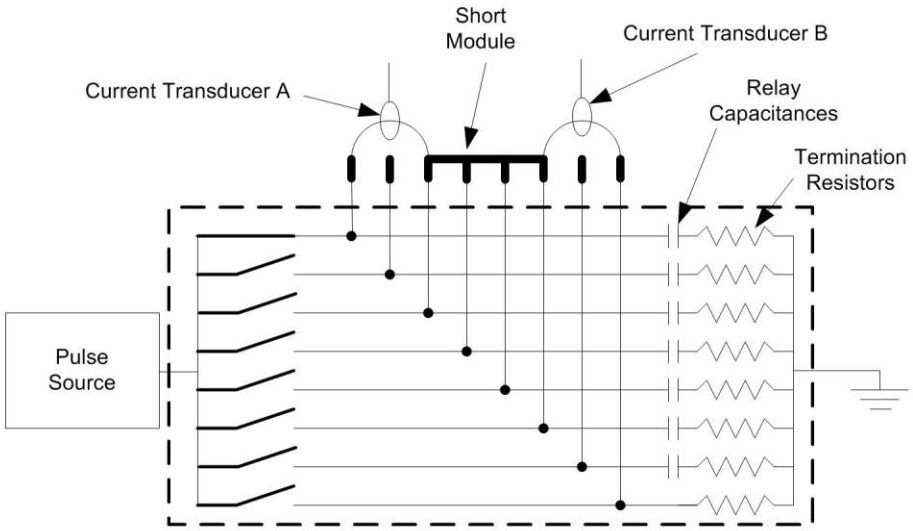

Figure 6: Modified HBM schematic showing relay capacitance and termination resistors

The circuit for the simulation is shown in Figure 7. The 1pF capacitor and 5μH inductor simulate realistic parasitics in the HBM simulator pulse source. [8] The 1500 Ω HBM resistor has been reduced to 1425 Ω to account for the 75 Ω termination resistor. If n +1 pins are shorted together by the device under test there are n parallel parasitic current paths. Each of these paths is a series combination of a single termination resistor and an open relay capacitance. The n parallel paths can be replaced by a series combination of a single resistor of value 75Ω/n, and a single capacitor, of value n×7.5pF.

Figure 8 shows a comparison of no parasitics and for 30 simulator channels shorted together by the device under test. Without the parasitic path the current looks very similar to the example in Figure 2. With the parasitic paths there is only a small increase in the peak current on the A Side. The increased peak current is due to the low high frequency impedance of the parasitic paths. The peak current measured on the B side is significantly reduced and there is a large increase in the rise time. Current through the parasitic path is very large until the relay matrix capacitance is charged. The parasitic current then reverses sign as the relay matrix capacitors discharge.

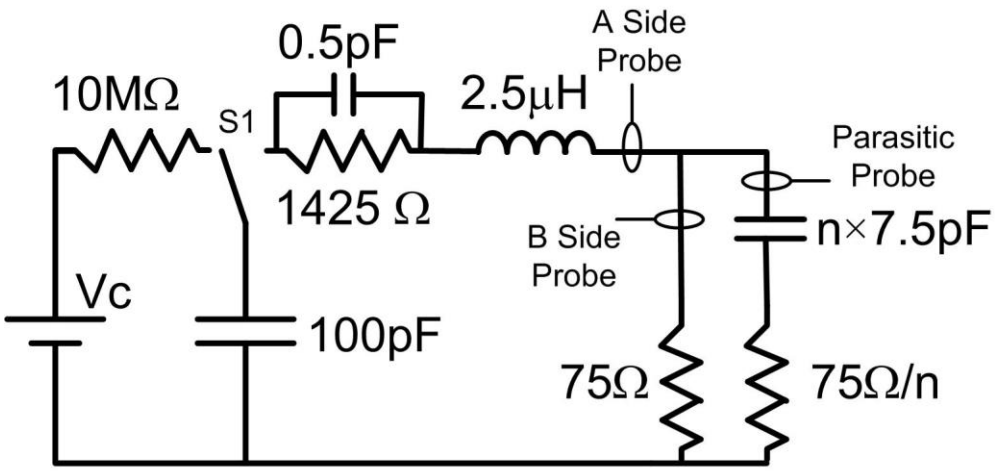

Figure 7: Schematic for circuit simulation

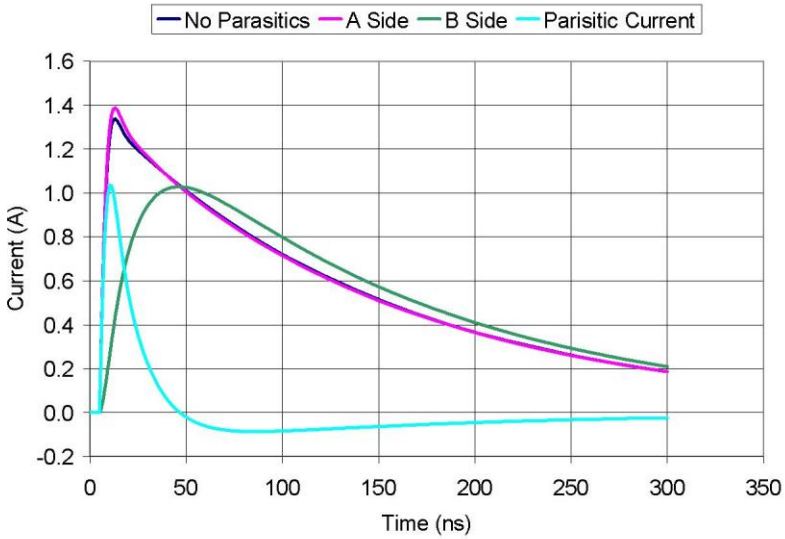

Figure 8: Simulated HBM waveforms with and without parasitic paths for a device under test with 30 shorted pins

How an integrated circuit is affected by simulator parasitics will vary from circuit to circuit. Circuits that are damaged by peak current may exhibit a higher HBM passing level, due to the simulator parasitics. Protection strategies that rely on a fast transient to turn protection circuits on may not work as intended during HBM testing. [6] A recent study by one equipment manufacturer has shown how simple spacers inserted between the test board and the simulator's relay matrix can greatly reduce parasitic effects. [9] The same study also showed that, at least for some circuits, the A side current pulse is more important than the B side pulse in determining device failure. It is important to note that no field failures have been linked to improper testing due to simulator parasitics.

HBM Qualification Levels

For many years 2000V has been the generally accepted value for passing the HBM ESD test. In recent years, with advanced integrated circuit technologies with smaller feature size, it has become more difficult to reach 2000V HBM. The result has been costly redesigns and delays in the introduction of new products. During the same period the ability to control ESD events in the manufacturing process has made the handling of products with HBM levels even below 500V routine.

The Industry Council on ESD Target Levels was formed in 2006 to determine the ESD robustness needed in today's manufacturing environment. The council is made up of ESD experts from a broad cross section of integrated circuit manufacturers, test system manufacturers and other interested parties. In 2007 the council released a white paper recommending that a 1000V HBM level was more than adequate to ensure that electrical components can survive the manufacturing process. [10]

Summary

The migration of HBM testing to more advance integrated circuits has not been without its challenges. Integrated circuit advances required the development of automated HBM simulators, allowing the testing of complex circuits. Over the years, problems such as the trailing pulse and pre pulse voltage have prompted modifications to some of the test systems. Today, the industry struggles with excessive test time, wear out and unintended interactions between the test system and the device being tested. Despite this, HBM remains a positive force in the electronics industry, preventing costly yield loss during manufacture.

Robert Ashton *is a senior protection and compliance specialist at ON Semiconductor, and can be reached at Robert.Ashton@onsemi.com.*

References

1. JEDEC, "JESD22-A-114D, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) Component Level," 2006
2. ESD Association, "Standard Test Method for Electrostatic Discharge (ESD) Sensitivity Testing: Human Body Model (HBM) Component Level," 2000.
3. R. Gaertner, R. Aburano(1), T. Brodbeck, H. Gossner, J. Schaafhausen, W. Stadler, F. Zaengl, "Partitioned HBM Test - A New Method To Perform HBM Tests On Complex Devices", EOS/ESD Symposium 2005, pg 178.
4. C. Duvvury et. al., "Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers," EOS/ESD Symposium, 2004, pg 132.
5. R. Ashton and E. Worley, "Pre Pulse Voltage in the Human Body Model," EOS/ESD Symposium, 2006, pg 326.
6. H. Kunz, "The Effect of High Pin-Count ESD Tester Parasitics on Transiently Triggered ESD Clamps," EOS/ESD Symposium, 2004, pg 146.
7. M. Chaine et.al., "HBM Tester Parasitic Effects on High Pin Count Devices with Multiple Power and Ground Pins," EOS/ESD Symposium, 2006, pg. 354.

8. K. Verhaege et.al., “Analysis of HBM ESD Testers and Specifications Using a 4th Order Lumped Element Model”, EOS/ESD Symposium, 1993, pg 129.
9. R. Given et.al., “Sudy of the Impact of Non-selected I/O Pins during HBM Test using ZapMaster Mk.2”, September 2007, http://www.thermo.com/eThermo/CMA/PDFs/Product/productPDF_2810.pdf.
10. Industry Council on ESD Target Levels, “White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements,” http://www.esdtargets.blogspot.com/.