Challenges in Testing

Pre-Pulse Voltage in the HBM ESD Model

Robert Ashton, ON Semiconductor

Dynamic clamps have become very popular in the last few years for providing ESD robustness for integrated circuits. [1] They have a number of advantages which will be described below.

Several years ago, a pattern emerged in the human body model (HBM) testing of dynamic clamp protected circuits. Circuits with moderate or high leakage were protected very well by dynamic clamps, but circuits with very low leakage would often fail at lower than expected values. It appeared that the dynamic circuits were not functioning as designed. Voltage measurements, prompted by the trailing pulse HBM simulator issues discovered by Texas Instruments, [2] revealed an unexpected voltage across the dynamic clamps before the HBM current pulse if the circuit leakage was very low.[3] (Note: an HBM simulator is a test instrument that performs a simulated ESD event on an electronic component. It is not a computer program.)

This article will explain the origin of this pre-pulse voltage (PPV), describe the working and advantages of dynamic clamps, explain how the PPV prevents operation of the dynamic clamp, relate how the PPV in an HBM simulator relates to real world ESD stress, discuss how the ESD standards have dealt with the PPV issue, and what concerns should remain about the PPV for ESD test engineers and ESD designers.

PPV Origin

The basic HBM schematic is shown in Figure 1. A 100pF capacitor is charged from a high voltage power supply, and a relay, S1, initiates the HBM stress pulse through a 1500Ω resistor to the device under test (DUT). The HBM current pulse has a 2 to 10 rise time and a 150ns exponential decay, assuming the DUT resistance is much less than 1500Ω, as illustrated in Figure 2.

Figure 3 shows measurements of the PPV. The DUT has been replaced with a 10V Zener diode, and the voltage across the diode has been measured alone and with 1MΩ and 10kΩ resistors in parallel to simulate varying degrees of leakage, as illustrated in Figure 1. The HBM schematic does not suggest any voltage across the device before the current pulse. Relays, however, are not perfect circuit elements, and their physical properties will differ from an ideal switch.

In the original PPV paper [3] two physical mechanisms were proposed that might explain the PPV. The first was that, as the relay closed, gas in the relay would start to ionize, but not enough to trigger the full scale avalanche that creates the HBM current pulse. The ionization current could charge the capacitance of the DUT and parasitic capacitance of the HBM simulator, creating the observed PPV.

The second proposal was that the relay S1 represents a variable capacitance as it closes. A schematic for this model is shown in Figure 4. (The capacitor C_{DUT} includes not only the DUT capacitance but also parasitic capacitance in the HBM simulator.) The model assumes a starting condition with the 100pF C_{HBM} capacitor charged to the HBM voltage. Voltage across the DUT is assumed to be 0V. The relay S1 is open with the relay elements far apart, such that the relay capacitance, C_{S1}, is low. Under these conditions, the voltage across C_{S1} must be equal to the HBM voltage.

As the relay closes, the relay elements get closer together and the capacitance C_{S1} increases. As the capacitance increases, more charge is needed to maintain the HBM voltage across the relay. On one side, the charge must come from the 100pF capacitor, slightly lowering the voltage across C_{HBM}. On the other side the charge must come from the DUT. For very large values of R_{DUT}, some of the charge must come from C_{DUT}. This increases the voltage across C_{DUT}, resulting in a PPV. Measurements by Barth et. al. [4] using vacuum relays, which are not subject to the ionization mechanism, proved that the PPV was caused by capacitance change within the relay as it closed.

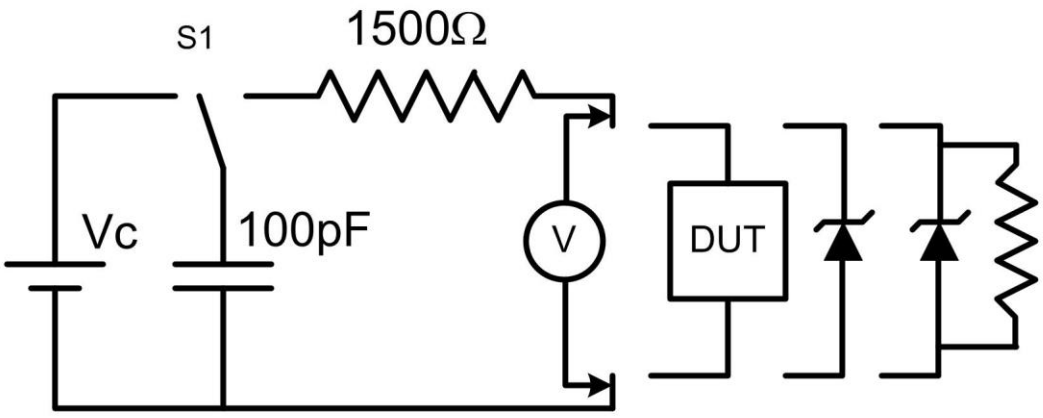

Figure 1: Basic HBM schematic showing the location of the device under test, the positioning of the Zener diode and Zener diode with parallel resistors as well as the location of the voltage probe during measurement of the PPV

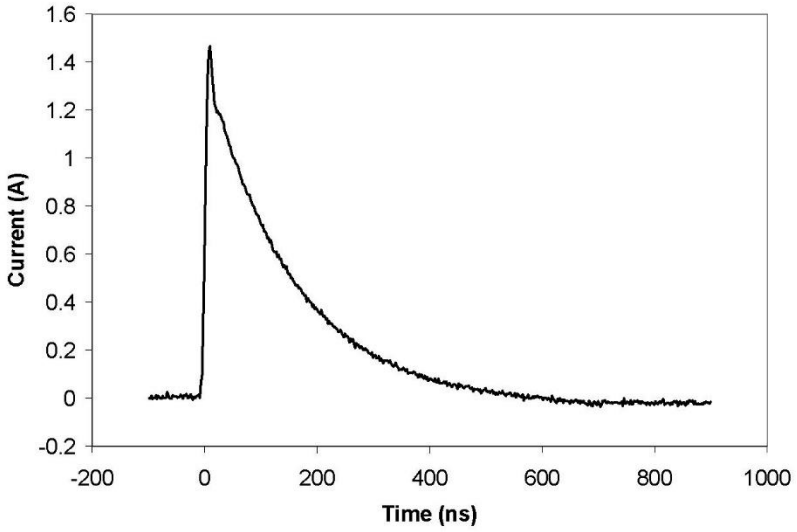

Figure 2: Measured HBM waveform for 2000V into a short

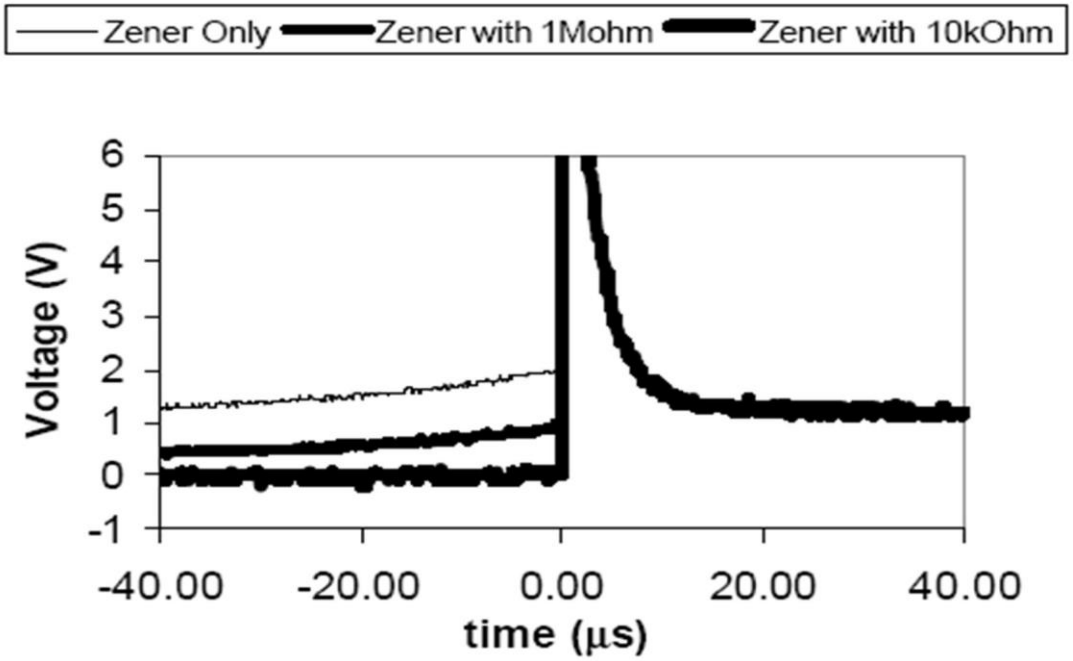

Figure 3: PPV measured across a 10V Zener diode and with 1MΩ and 10kΩ across the Zener

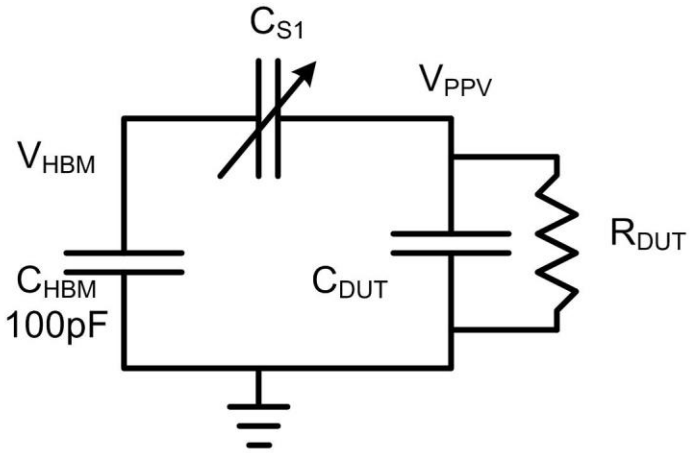

Figure 4: Schematic for model of PPV due to relay capacitance change

Dynamic ESD Clamps and PPV

A sample dynamic ESD clamp, often called a BigFET, is shown in Figure 5. The clamp is placed between power and ground. With steering diodes to power and ground on inputs and outputs, and an ESD diode between VDD and VSS, the BigFET can provide a full HBM protection strategy. In its on state, the BigFET's large nMOS can conduct the full HBM current pulse without damage, and maintain the VDD to VSS voltage within a safe range.

The inverter chain and RC circuit are designed to keep the large nMOS off during normal operation, but turn on the large nMOS during an ESD event. While power is applied to the circuit, node A in Figure 5 is held high and, due to the three stages of inverter, node B will be held low, keeping the large nMOS device off.

The HBM ESD test is intended to determine an integrated circuit's ESD robustness before it is inserted on a circuit board. The HBM test is therefore performed on an unpowered integrated circuit. Consider a positive ESD event on VDD with respect to VSS. The rapid rise of VDD versus VSS caused by the ESD event will result in node A staying close to VSS for an RC time constant. With node A held low, the three stages of inverters will hold node B high, turning on the large nMOS device, providing a safe path for the HBM current stress. ESD stresses that result in negative stress between VDD and VSS are handled by forward biased diodes, typically formed by nWell to substrate diodes.

Dynamic clamps have two main advantages. They protect without relying on avalanche breakdown, and their behavior can be predicted using Spice simulation.

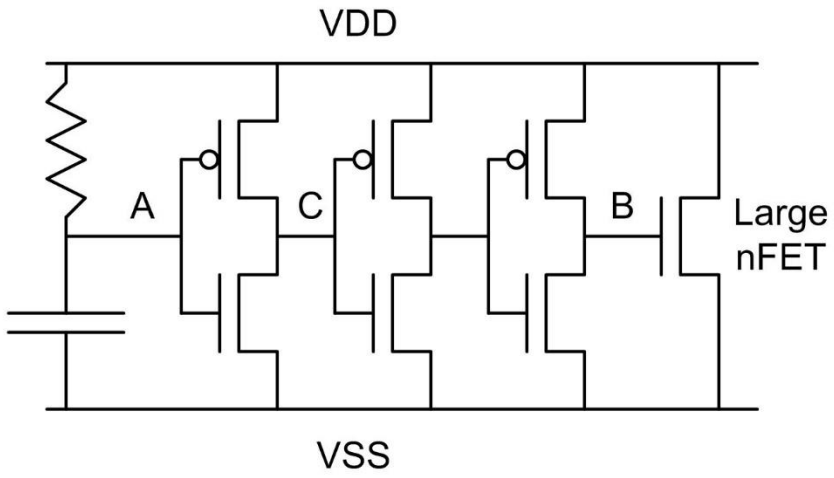

Figure 5: Schematic of a typical dynamic ESD clamp

The failure of dynamic clamps to function due to the PPV on low leakage circuits is easy to explain. The PPV develops while the relay S1 in Figure 1 is closing, which takes many μs as shown in Figure 3. This is much longer than the RC time constant in any reasonable dynamic clamp circuit.

When the HBM pulse in the simulator occurs, node A may already be well above the nMOS threshold voltage. A further increase in VDD caused by the HBM current pulse will not turn off the first stage nMOS device. The increase in VDD will result in a turn on of the pMOS device in the first stage. The voltage at the input to the second stage of the inverter chain, node C, will be the result of a battle between the first stage's n and p channel devices. This is a battle that the nMOS device often wins, keeping node C, and therefore node B, low and the large nMOS in an off state.

PPV and the Real World

The discovery of the PPV presented a dilemma: is this a phenomena that is unique to an ESD simulator, or is it a problem in the real world? Asked another way, do we need to fix the HBM simulator, or do we need to fix or not use dynamic clamps on low leakage circuits?

Early measurements indicated that the PPV is a real world issue. PPV was measured when a charged person touched a Zener diode mounted on a current probe. In fact, the measured voltage across the Zener diode touched by a charged person was even higher than observed on the HBM simulator.[4] The explanation of the PPV for a real world situation is the same as in the simulator. The charged human has a capacitance to their surrounding, about 100pF, and forms a small, variable, capacitance between their finger and anything he or she touches as the finger approaches the object.

However, the original real world measurements did not represent the real world in one significant way. The geometry did not accurately replicate a person touching an integrated circuit. In the "real world" events, the Zener was housed in a flat surfaced fixture. The capacitance between the person and the Zener was therefore a flat surface to

a rounded finger. This creates a much larger capacitor than would occur between a finger and the small pins of a modern integrated circuit. To investigate this, a more realistic real world simulation was needed.

Several simulated packaged integrated circuits were built from circuit board material and Zener diodes. A schematic is shown in Figure 6 and photographs are shown in Figure 7. The Zener diodes simulate the protection circuitry on an integrated circuit. They have high input impedance between 0 and 10 V and low resistance below and above those voltages. Wires attached to the cathode end of the diodes allowed measurement of the voltage on the solder balls or pins of the simulated packages.

The simulated packages were fitted with a 3mm threaded screw that could fit into the center of an IEC 61000-4-2 compliant current sensor. The current sensing target was used solely to trigger an oscilloscope and provide a ground point. The remaining 3 channels of the oscilloscope could be used to monitor the voltage on the package pins.

Rather than use a charged person's finger, an ESD gun in air discharge mode with a round tip was used. To make measurements the ESD gun was set to a voltage, the ESD gun's trigger was pulled, charging the tip of the gun, and the gun was moved toward the package pins until an arc occurred, triggering the oscilloscope.

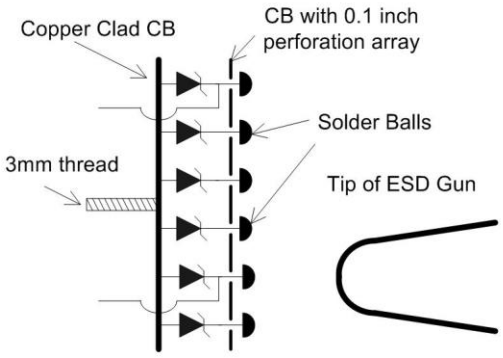

Figure 6: Schematic of simulated integrated circuit

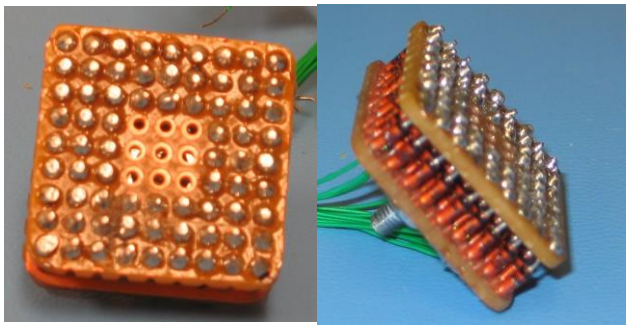

Figure 7: Photos of simulated integrated circuit

Measurements on the simulated ball grid array (BGA) packages showed that the PPV was indeed much lower than for the geometry with a person's finger touching a flat surface. The resulting PPV was so much smaller that the 10MΩ input impedance of the oscilloscope probes that had been used had to be augmented with 100MΩ resistors, so that the PPV could be easily observed.

The simulated BGA packages were not suitable for determining a quantitative measurement of the PPV as a function of pin size. A second set of simulated packages was developed with a variety of pin sizes made from wires of various diameters, as well as a flat surface control and a pin made out of thin sheet metal. The measured results are shown in Figure 8.

The measurements show that, for a flat surface, the PPV was enough to raise the voltage all the way to the breakdown voltage of the Zener diode. At smaller geometries, similar to those in modern high pin count packages, the PPV was well below a volt.

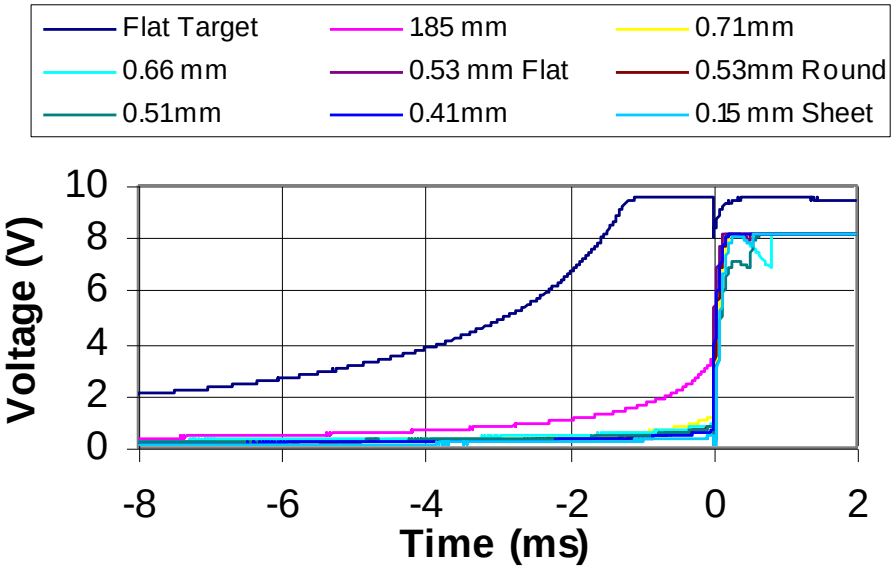

Figure 8: Measured PPV for different geometry pins

PPV and HBM Standards

The measurement on simulated packages showed the PPV not to be as serious a problem in a real world situation as was originally feared. It is only for unusual geometries, very high impedance, and low capacitance situations where PPV is likely to result in the failure of dynamically triggered circuits to function. For this reason, the JEDEC HBM standard [5] was modified to allow as low as a 10kΩ resistor to be placed across the pulse source during HBM stress. This resistance allows the charge to bleed off of the integrated circuit pin being stressed, but will not carry any significant current during the actual HBM current pulse.

The Electrostatic Discharge Association (ESDA) is taking a more cautious approach on their HBM standard [6]. An appendix has been added, showing how to measure the PPV, but they have not gone so far as to allow the PPV to be entirely removed from the HBM simulator.

Conclusion

The PPV has been shown to be a cause for failure of dynamically triggered ESD protection circuits in HBM simulators, but measurements on specially designed simulated integrated circuit packages have shown that it is not a severe a problem in real world situations. For this reason, the JEDEC HBM standard has been modified to allow HBM simulators to remove the PPV with a bleed resistor. There are, however, many HBM simulators still in use throughout the world that do not have this modification in place. There can also be, under rare conditions, circuits that may fail to work in a real world situation due to the PPV effect.

Robert Ashton *is a senior protection and compliance specialist at ON Semiconductor, and can be reached at Robert.Ashton@onsemi.com.*

References

[1] E. Worley, R Gupta, B. Jones, R. Kjar, C. Nguyen, and M. Tennyson, "Sub-Micron Chip ESD Protection Schemes which Avoid Avalanching Junctions" in EOS/ESD Symposium Proceedings, 1995, pp. 13-20, Phoenix, AZ, September 1995.

[2] C. Duvvury, R. Steinhoff, G. Boselli, V. Reddy, H. Kuntz, and R. Cline; "Gate Oxide Failures Due to Anomalous Stress from HMB ESD Testers" EOS/ESD Symposium Proceedings; 2004 pp132-140.

[3] R. Ashton, B. Wier, G. Weiss, and T. Muse, "Voltages Before and After HBM Stress and Their Effect on Dynamically Triggered Power Supply Clamps", EOS/ESD Symposium Proceedings, pp 153-159, 2004.

[4] J. Barth, R. Ashton, E. Worley, and J Richner; "Voltages Before and After Current in HBM Testers and Real HBM", EOS/ESD Symposium; pp 141- 150, 2005.

[5] JEDEC Standard JESD22-A114E, “Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)”, January 2007.

[6] ANSI/ESD STM5.1-2007, “For Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) Component Level” Electrostatic Discharge Association, 2007.