System Level ESD Testing Part I: The Waveforms

Introduction

The user of an electronic product, whether it is a cell phone, a computer or a game console, is justifiably upset if they touch their device, feel a small ESD discharge and then find their prized possession not working, either temporarily or permanently. The user will not care that they were charged up to many thousands of volts when they touched the product, or that the current into the device was several amps. They want the product to work first time, every time. To prevent these kinds of problems test standards have been developed to test systems for ESD robustness. The best known of these is the IEC 61000-4-2 standard but there are others such as ISO 10605 and SAE J1113-13 for testing of automotive components. Testing with these standards allows one to find and correct vulnerability of products to ESD stress.

While testing systems for ESD robustness is done extensively, the nature of the tests are often misunderstood. This is especially true for engineers that are more familiar with the classic device level tests of Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) applied to integrated circuits. This is the first in a series of articles on system level ESD testing that will try to improve the level of understanding of system level testing. This first article will explain the intension of ESD tests for both devices and system level, and then discuss the device level and system level stress waveforms. Subsequent articles will describe the system level testing in more detail and the issues that need to be considered when designing a system level test.

Purpose of Tests

The purpose of system level and device level testing is different. System level test is intended to insure that finished products can survive normal operation. It is not assumed that the user of the product will take any ESD precautions to lower stress to the product. The purpose of traditional ESD testing of integrated circuits is very different. HBM, MM and CDM tests are intended to insure that integrated circuits survive the manufacturing process. For example, an integrated circuit needs to survive saw apart from the wafer, packaging, final test, shipment to a board assembly facility, placement on a circuit board with automatic pick and place machinery and the solder process. All of these processes are done in a controlled ESD environment that limits the level of ESD stress that the device is exposed to. Even when the device is on a circuit board it is expected that ESD precautions such as shipment in ESD safe packaging material must be taken to minimize stress to the board. Once the board is in a system ESD precautions are no longer assumed. A system level ESD test can therefore be expected to be a much more sever test than that intended for an integrated circuit.

(Consider paragraph or side box that deals with exceptions to the device getting protection from the system or board.)

The Nature of ESD Tests

ESD tests are intended to simulate real world events, with different test standards intended to cover different situations. The HBM device standard is intended to simulate a person becoming charged and discharging from a bare finger to ground through the circuit under test. The MM is intended to simulate a charged machine, such as a pick and place machine, discharging through the device to ground. CDM simulates an integrated circuit becoming charged and discharging to a grounded metal surface. System level tests, such as IEC 61000-4-2 and ISO 10605 replicate, similar to HBM, a charged person discharging to a system. The only conceptual difference between the IEC 61000-4-2 standard and device level HBM is that for the system test it is assumed that the person is holding a metal object such as a key or screwdriver. This, as we shall see produces a very different waveform.

Device Level ESD Waveforms

We will now discuss the individual models and the stress waveforms that are associated with each standard. Each of the standards is characterized by a capacitor that is charged and a discharge path. We will start with the HBM standard, since it is the most popular device level test. A person's capacitance to their surroundings is approximately 100pF. and the HBM standard uses this value to represent a person. The discharge path includes a person's skin resistance and the resistance of the spark, which has been approximated as 1500Ω. The traditional circuit diagram for HBM is shown in Figure 1. An actual HBM current waveform is shown in Figure 2.

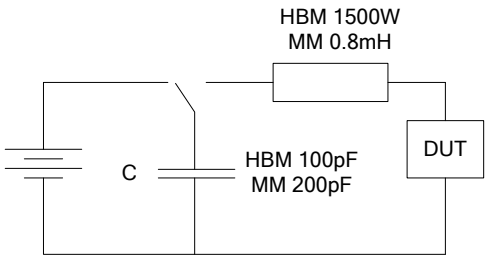

Figure 1 Basic circuit diagram for HBM and MM

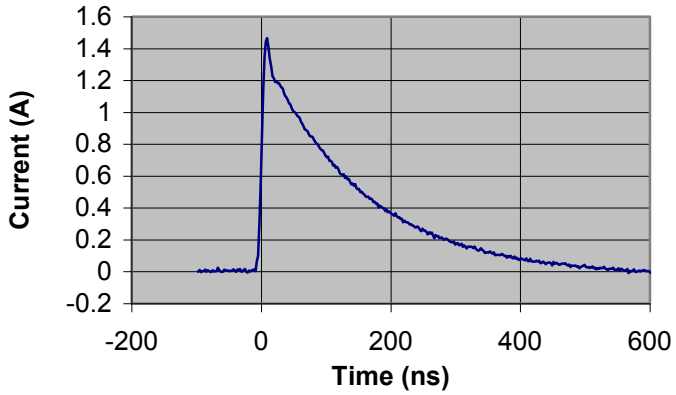

Figure 2 2000V HBM Current waveform into a short

Note that a characteristic of HBM, and all of the ESD standards, is that the ESD stress is specified by a current waveform into a defined load. The compliance of the waveform to the standard is determined by waveform parameters such as peak current, rise time, percent ringing and decay time. The values of the resistors, capacitors, and inductors in the circuit diagrams and are in fact not specified in the standards, only the current waveforms, only "nominal" values for the circuit elements are in the standards. A feature of all of the standards is that the basic circuit diagram presented for the model will not produce the specified waveforms. There are always "parasitic" circuit elements that are needed to create the specified waveforms. The deviation of the waveforms from the waveform predicted by the simple schematics is on purpose. All real world test systems have parasitics that can not be avoided. Standards must reflect systems that can be built in the real world.

The machine model has a very similar circuit diagram as HBM and is shown in Figure 1. The capacitor value is increased to 200pF and an approximately 0.8μH inductor replaces the 1500Ω resistor from HBM. The inductor is not specified in the standards but is needed to produce the required oscillatory MM waveform. Figure 3 shows an actual, in specification, waveform for MM. Note that even though the charging voltage for the waveform shown in Figure 3 is a tenth that of the HBM example the peak current is considerably higher.

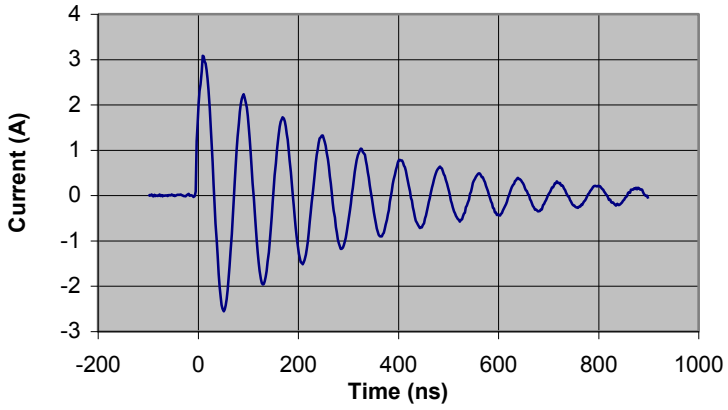

Figure 3 200V MM waveform into a short

CDM is substantially different from HBM and MM. There is no capacitor even nominally specified in the standard. This makes sense because the CDM discharge simulates a charged integrated circuit being discharged to a metal surface. The capacitor is the device's capacitance to its surroundings. There are several charged device test methods but one of the most popular is the Field Induced CDM (FCDM). A simplified diagram of a field induced CDM tester is shown in Figure 4. The tester consists of a Field Plate that can be raised to a high voltage. The field plate is covered with a thin insulator. A circuit placed pin side up on the field plate insulator (dead bug position) will have a capacitance to the field plate that is dependent on the size and geometry of the circuit being tested. This is the capacitor that will be charged. Over the field plate is a grounded plate with a spring loaded "Pogo Pin". The Pogo Pin is electrically connected to the ground plane with a low inductance circular 1Ω resistor as well as to a 50Ω cable that can be used to capture the CDM current waveform. The Ground Plane and the Field Plate can be moved relative to each other under computer control so that the Pogo Pin can be brought in contact with the pins of the device on the Field Plate.

If the capacitance between the integrated circuit and the field plate is much larger than the capacitance of the integrated circuit to the ground plane and any other parts of the test system, the potential of the integrated circuit will track the potential of the field plate. The test procedure is to place the uncharged integrated circuit on the insulated Field Plate and then slowly raise the potential of the Field Plate, and consequently the potential of the integrated circuit, to a high voltage. Touching an IC pin while it is at high potential with the Pogo Pin will ground the IC. This will occur very quickly and will result is a very short duration high current pulse. The current level of this event is shown for 500V on a JEDEC small calibration module in Figure 5. The current pulse is over in about 2 ns. This compares to the100s of ns time scales for HBM and MM.

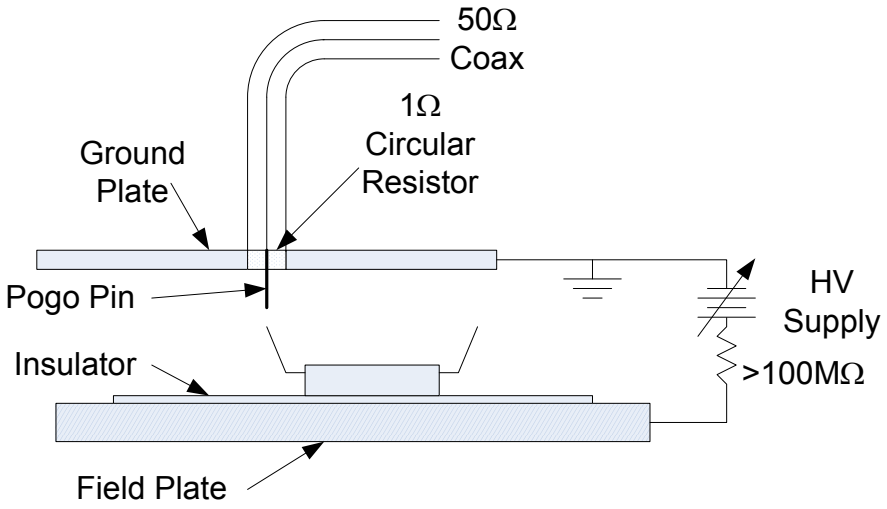

Figure 4 Diagram of a Field Induced CDM ESD Tester

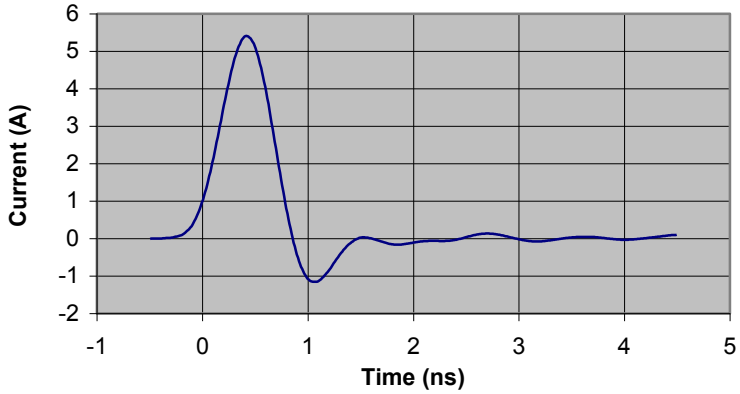

Figure 5 Field Induced CDM waveform of a small JEDEC Module at 500V

System Level ESD Waveforms

As discussed earlier the IEC 61000-4-2 stress is intended to simulate a person discharging into a system while holding a metal object such as a key. Touching with a metal object suggests that at least for the early part of the discharge there will be very little resistance other than the arc resistance of the discharge. The circuit diagram for the IEC pulse source as in the specification is shown in Figure 6 and a schematic view of the waveform, as well as the parameter to characterize the waveform are shown in Figure 7. The IEC waveform uses a C1 capacitor with a nominal value of 150pF Capacitor, 50% larger than the HBM value, and an R1 resistor of nominal value 330Ω, only 22% of the HBM value. This suggests that the IEC waveform will have a higher peak current and faster decay time than an HBM waveform. The IEC waveform, however, is not just different in magnitude; the waveform has a distinctly different shape. This can be easily seen by comparing the HBM waveform in Figure 2, the schematic IEC waveform in

Figure 7 and a sample IEC compliant waveform shown in Figure 8. The IEC waveform has a very fast, large amplitude current spike at the beginning of the waveform. The circuit diagram shown in Figure 6, as it is presented in the IEC standard, can not create the waveform that the standard calls for. A superficial examination of the IEC and HBM circuit diagrams often leads people to expect the waveforms to be similar. The movement of the relay from one side of the resistor to the other, and the presence of parasitic capacitance, results in a significant change in the waveform. A more realistic circuit diagram is shown in Figure 9. (Pommerenke and Aidam[i] give a more detailed circuit diagram useful for waveform simulation.) The placement of the relay on the device under test side of the resistor means that any parasitic capacitance on the device side of the resistor will be charged before the relay closes. When the relay closes the capacitance C2 will discharge into the device under test with only parasitic inductance and resistance to limit the current. This produces the large initial current spike in the IEC waveform. The presence of the spike in the required IEC waveform **requires** the parasitic capacitor C2. In contrast HBM parasitic capacitance on the device under test side of the 1500Ω resistor will not be charged before the relay closure and no initial current spike is produced.

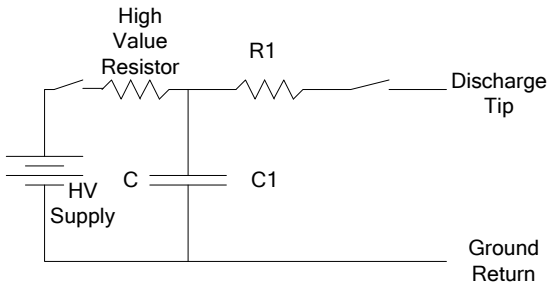

Figure 6 IEC 61000-4-2 schematic as shown in specification

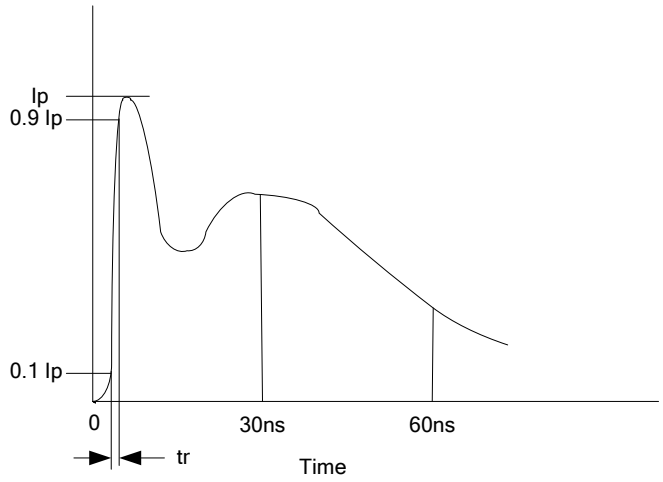

Figure 7 Schematic diagram of the IEC waveform and the parameters used to characterize the waveform

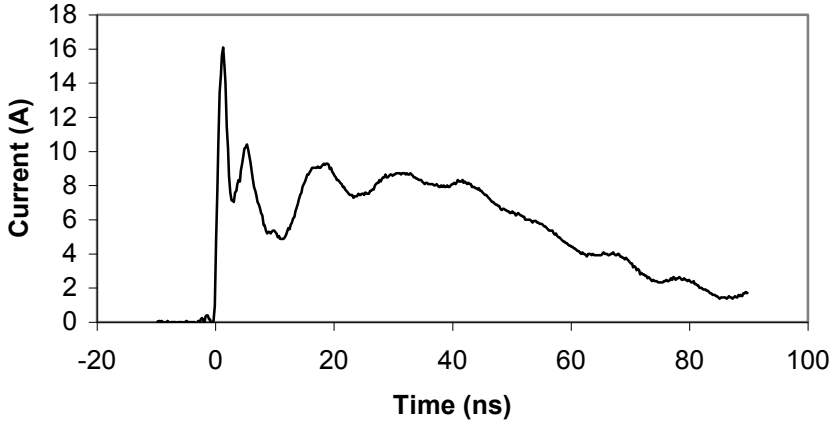

Figure 8 Waveform from an IEC compliant ESD gun at 4000V

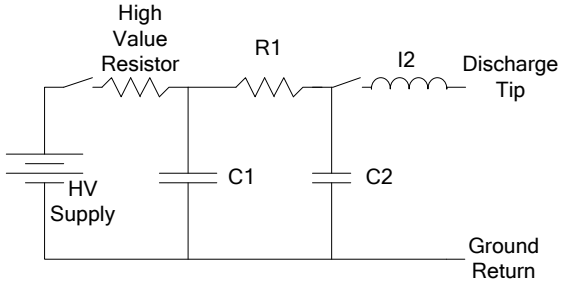

Figure 9 More realistic IEC 61000-4-2 schematic

The dominance of the “parasitic” capacitor C2 on the initial current pulse is easily illustrated if the IEC 61000-4-2 waveform is compared with the waveforms for the automotive system level test ISO 10605. The ISO test uses the same type of ESD gun as the IEC test but the resistor R1 is changed from 330Ω to 2000Ω while the 150pF C1 capacitor is either left at 150pF or changed to 330pF, depending on the system being tested. Waveforms from the same ESD gun with the different R1 and C1 values at 4000V are shown in Figure 10. The initial peak is identical because it is dominated by C2 and I2 but after the first 5 to 10 ns the waveform starts to depend on C1 and R2. The difference between the two ISO waveforms only becomes obvious at longer times such as in Figure 11 for stress at 8000V.

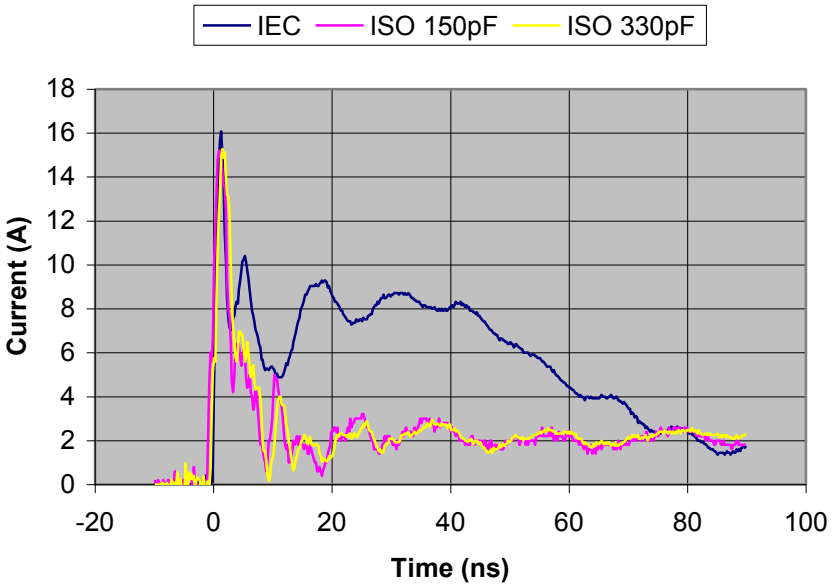

Figure 10 Comparison of ISO 61000-4-2 waveform with ISO 10605 waveforms with both 150pF and 330pF capacitances at 4000V

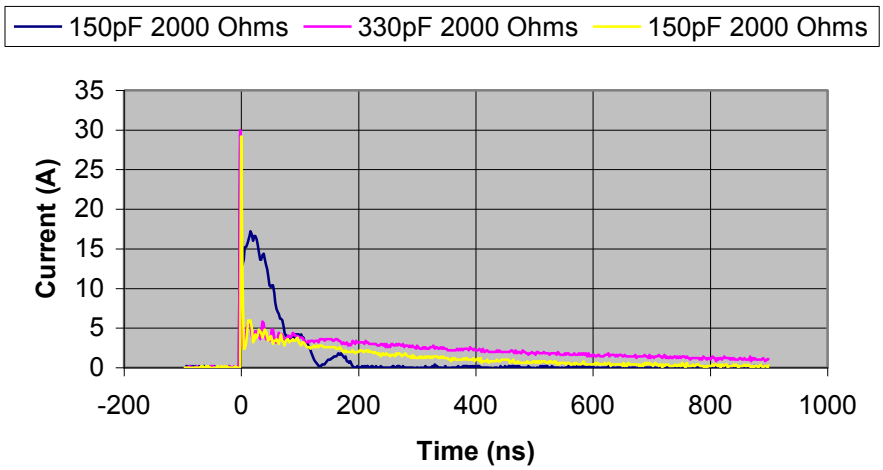

Figure 11 Comparison of ISO 61000-4-2 waveform with ISO 10605 waveforms with both 150pF and 330pF capacitances at 8000V

System and Device Waveform Comparison

The difference between system and device level stress becomes obvious when the current waveforms are displayed on the same plot as they are in Figure 12, and with an expanded time scale in Figure 13. 500V CDM and 2000V HBM are the most common target levels for product acceptance for ESD tests on integrated circuits and it is often hard to obtain these levels of robustness especially on modern high speed circuits. 2000V IEC stress is however the **minimum** test level specified for system testing. Even with this minimum level of stress for IEC the system level currents are several times larger than the HBM stress, although the HBM stress does continue for somewhat longer than the IEC stress. The peak CDM current comes closer to the peak current of the IEC stress and has similar rise time, but the duration of the IEC stress almost 2 orders of magnitude longer. In some ways the IEC system level stress looks similar to a combination of the fast rise time peak of CDM and the longer lasting current from HBM. As the stress levels for system level test are raised from the minimum level of 2000V to 8000V for IEC contact discharge the higher level of stress for system level testing becomes even greater.

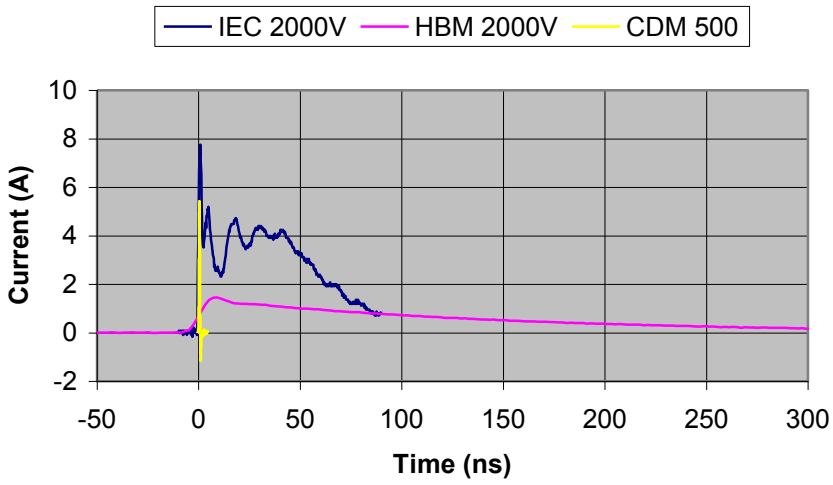

Figure 12 Comparison of IEC, HBM and CDM waveforms

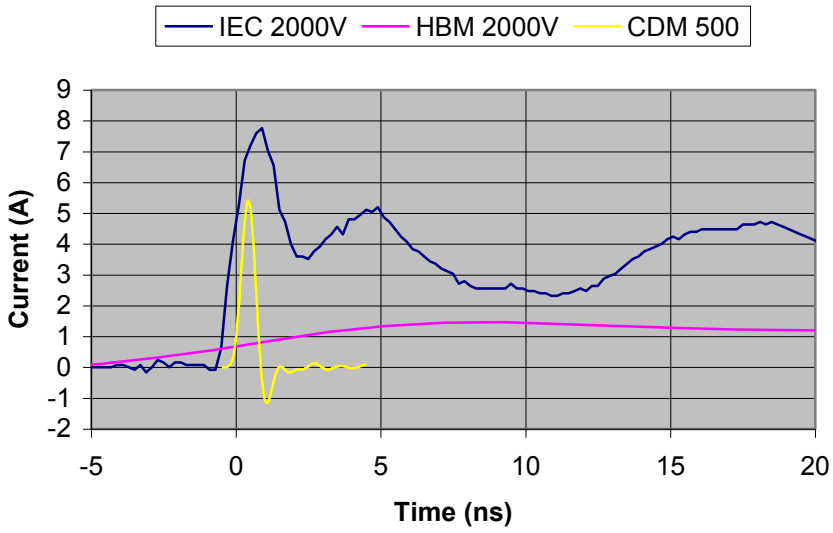

Figure 13 Comparison of IEC, HBM and CDM at an expanded time scale

Summary

The current waveform stresses for some of the most common device and system level tests have been presented. It has been shown how system level testing, especially for IEC 61000-4-2 is much more sever than device level test; combining both the fast rise time and high peak current of a CDM event with the more long lasting currents of the HBM test. Knowledge of the waveform, no mater how complete, does not fully define the test. This is especially true for system level ESD testing. In order to upset or damage a system the stress must reach a sensitive component. The stress must also be done in a way that approximates a real world event or the test does not provide value. In subsequent articles in this series the details of system level ESD test will be discussed.

[i] D. Pommerenke and M. Aidam, "To what Extent do Contact Mode and Indirect ESD Test Methods Reproduce Reality?" 1995 EOS/ESD Symposium, pp. 101-109.